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NOBUHIRO ITO ET AL.	)	
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For: ELECTRON BEAM APPARATUS AND SPACER	) :	February 12, 2004

The Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF SWORN TRANSLATION OF PRIORITY APPLICATION

Sir:

Applicants submit herewith a sworn English translation of Japanese Application No. JP 10-285759, filed October 7, 1998, from which this application claims priority.[1/] The filing of this sworn translation removes reference 6,222,313 (Smith), which was filed on December 11, 1998 and issued on April 24, 2001, as a reference against the claims supported by the Japanese application.

All of the pending claims are believed to be patentable for the reasons given in the Remarks section of the Amendment filed on November 5, 2001. Accordingly,

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1/ A Declaration stating that the English translation of Japanese Application No. JP 10-285759 is accurate is submitted herewith.

Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

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This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: October 7, 1998

Application Number: Japanese Patent Application No. 10-285759

Applicant(s): CANON KABUSHIKI KAISHA

October 29, 1999

Commissioner,
Patent Office Takahiko Kondo

(Seal)
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[List of Filed Materials]

[Material]	Specification	1
[Material]	Drawings	1
[Material]	Abstract	1

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10-285759

[Name of the Document] Specification

[Title of the Invention] Electron Beam Apparatus and Spacer

[Claim(s)]

[Claim 1] An electron beam apparatus comprising an electron source, a plate facing said electron source, and a spacer installed between said electron source and said plate,

when the incident angle dependency of secondary electron emission coefficient on the spacer surface is small and incident energy of primary electron to said spacer is below the maximum,

[Numerical Formula 1]

δ_θ, δ_0

are respectively the second electron emission coefficient against the primary electron at incident angle θ and 0 degrees,

[Numerical Formula 2]

$$\frac{\delta_\theta}{\delta_0} = \frac{1}{\cos\theta}\frac{1-\exp(-m_0\cos\theta)}{1-\exp(-m_0)} \qquad \text{General Formula (1)}$$

wherein the value of the incident angle multiplication coefficient of secondary electron emission coefficient m_0, which is a parameter is 10 or less.

[Claim 2] The electron beam apparatus according to claim 1, wherein the incident angle multiplication coefficient of secondary electron emission coefficient

m_0 is 5 or less.

[Claim 3] The electron beam apparatus according to claim 1 or 2, wherein said spacer comprises a spacer substrate provided with an uneven geometry at least on a part of its surface and a highly resistive film coating at least a part of said spacer substrate, the average thickness of said highly resistive film being smaller than the difference between the maximum and minimum values of the uneven geometry of said spacer substrate.

[Claim 4] The electron beam apparatus according to claim 3, wherein the uneven geometry on the surface of said spacer substrate is formed in such a direction that the incident angle dependency of said secondary electron emission coefficient is reduced for any of the orbits of the electron beam from said electron emission device as well as of the electron beam reflected on said face plate.

[Claim 5] The electron beam apparatus according to claim 3 or 4, wherein the uneven geometry on the surface of said spacer substrate is formed in at least two arbitrary directions.

[Claim 6] The electron beam apparatus according to any one of claims 3 to 5, wherein the average cycle W of the uneven geometry on the surface of said spacer substrate is 100 μm or shorter.

[Claim 7] The electron beam apparatus according

to claim 6, wherein the average cycle W of the uneven geometry on the surface of said spacer substrate is 10 μm or shorter.

[Claim 8] The electron beam apparatus according to any one of claims 3 to 7, wherein the average roughness of the uneven geometry on the surface of said spacer substrate is ranging from 0.1 μm to 100 μm.

[Claim 9] The electron beam apparatus according to any one of claims 3 to 8, wherein the uneven geometry on the surface of said spacer substrate consists of the cycles periods of at least two kinds of unevenness.

[Claim 10] The electron beam apparatus according to any one of claims 3 to 9, wherein the uneven geometry on the surface of said spacer substrate has a groove or hole formed by chemical or electrochemical corrosion treatment on the surface.

[Claim 11] The electron beam apparatus according to any one of claims 3 to 9, wherein the uneven geometry on the surface of said spacer substrate has a groove or hole formed by removing the surface partially using the spray treatment of a solid, liquid and particle group.

[Claim 12] The electron beam apparatus according to any one of claims 3 to 11, wherein the surface of said spacer substrate is provided with a porous glass or porous ceramic.

[Claim 13] The electron beam apparatus according to any one of claims 3 to 12, wherein the uneven geometry on the surface of said spacer substrate is formed by a roughed surface layer provided between said highly resistive film and said spacer substrate.

[Claim 14] The electron beam apparatus according to claim 13, wherein said roughed surface layer is provided by containing fine particles in a binder matrix dispersedly.

[Claim 15] The electron beam apparatus according to any one of claims 3 to 14, wherein said highly resistive film has a sheet resistivity of $10^5 [\Omega/\square]$ to 10^{12} $[\Omega/\square]$.

[Claim 16] The electron beam apparatus according to any one of claims 3 to 15, wherein said highly resistive film consists of nitride, oxide or carbide containing at least one kind of metal element carbon, silicon, or germanium.

[Claim 17] The electron beam apparatus according to any one of claims 3 to 16, wherein secondary electron emission coefficient of said highly resistive film measured under vertical incident conditions to a smooth surface formed on a smooth substrate is 3.5 or less.

[Claim 18] The electron beam apparatus according to any one of claims 3 to 17, wherein the surface of said highly resistive film has a high oxygen

concentration as compared with the inside thereof.

[Claim 19] The electron beam apparatus according to any one of claims 3 to 18, wherein said highly resistive film is formed by any one of the following methods: sputtering, vacuum deposition, wet printing, spraying, or dipping.

[Claim 20] The electron beam apparatus according to any one of claims 3 to 19, wherein said highly resistive film is connected to an electrode provided by said electron source and an electrode provided by said face plate via a low resistive film.

[Claim 21] The electron beam apparatus according to claim 20, wherein the surface resistivity of said low resistive film is lower than that of said highly resistive film by one digit or more.

[Claim 22] The electron beam apparatus according to any one of claims 1 to 21, wherein said electron emission device is a cold cathode device.

[Claim 23] The electron beam apparatus according to any one of claims 1 to 21, wherein said electron emission device has a conductive film containing electron emission portion between the electrodes.

[Claim 24] The electron beam apparatus according to any one of claims 1 to 21, wherein said electron emission device is a surface conduction electron emission device.

[Claim 25] The electron beam apparatus according

to any one of claims 1 to 24, wherein said face plate further has a target which produces an image when said accelerated electrons are irradiated.

[Claim 26] The electron beam apparatus according to claim 25, wherein said target is provided with a fluorescent substance.

[Claim 27] The electron beam apparatus according to any one of claims 1 to 26, wherein the voltage applied between said electron emission device and said anode is 3 kV or higher.

[Claim 28] A spacer, when the incident angle coefficient of secondary electron emission coefficient on the surface is small and incident energy of primary electron to said spacer is below the maximum,

[Numerical Formula 3]

δ_θ, δ_0

are respectively the second electron emission coefficient against the primary electron at incident angle θ and 0 degrees,

[Numerical Formula 4]

$$\frac{\delta_\theta}{\delta_0} = \frac{1}{\cos\theta}\frac{1-\exp(-m_0\cos\theta)}{1-\exp(-m_0)} \qquad \text{General Formula (1)}$$

wherein the value of the incident angle multiplication coefficient of secondary electron emission coefficient m_0, which is a parameter is 10 or less.

[Claim 29] The spacer according to claim 28, wherein the incident angle multiplication coefficient of secondary electron emission coefficient m_0 is 5 or

less.

[Claim 30] The spacer according to claim 28 or 29, comprising a spacer substrate provided with an uneven geometry at least on a part of its surface and a highly resistive film coating at least a part of said spacer substrate, the average thickness of said highly resistive film being smaller than the height difference between the maximum and minimum values of the uneven geometry of said spacer substrate.

[Claim 31] The spacer according to claim 30, wherein the uneven geometry on the surface of said spacer substrate is formed in at least two arbitrary directions.

[Claim 32] The spacer according to claim 30 or 31, wherein the average cycle W of the uneven geometry on the surface of said spacer substrate is 100 μm or shorter.

[Claim 33] The spacer according to claim 32, wherein the average cycle W of the uneven geometry on the surface of said spacer substrate is 10 μm or shorter.

[Claim 34] The spacer according to any one of claims 30 to 33, wherein the average roughness of the uneven geometry of the surface of said spacer substrate is ranging from 0.1 μm to 100 μm.

[Claim 35] The spacer according to any one of claims 30 to 34, wherein the uneven geometry on the

surface of said spacer substrate consists of the cycles periods of at least two kinds of unevenness.

[Claim 36] The spacer according to any one of claims 30 to 35, wherein the uneven geometry on the surface of said spacer substrate has a groove or hole formed by chemical or electrochemical corrosion treatment on the surface.

[Claim 37] The spacer according to any one of claims 30 to 35, wherein the uneven geometry on the surface of said spacer substrate has a groove or hole formed by removing the surface partially using the spray treatment of a solid, liquid and particle group.

[Claim 38] The spacer according to any one of claims 30 to 37, wherein the surface of said spacer substrate is provided with a porous glass or porous ceramic.

[Claim 39] The spacer according to any one of claims 30 to 38, wherein the uneven geometry on the surface of said spacer substrate is formed by a roughed surface layer provided between said highly resistive film and said spacer substrate.

[Claim 40] The spacer according to claim 39, wherein said roughed surface layer is provided by containing fine particles in a binder matrix dispersedly.

[Claim 41] The spacer according to any one of claims 30 to 40, wherein said highly resistive film has

a sheet resistivity of 10^5[Ω/□] to 10^{12} [Ω/□].

[Claim 42] The spacer according to any one of claims 30 to 41, wherein said highly resistive film consists of nitride, oxide or carbide containing at least one kind of metal element carbon, silicon, or germanium.

[Claim 43] The spacer according to any one of claims 30 to 42, wherein secondary electron emission coefficient of said highly resistive film measured under vertical incident conditions to a smooth surface formed on a smooth substrate is 3.5 or less.

[Claim 44] The spacer according to any one of claims 30 to 43, wherein the surface of said highly resistive film has a high oxygen concentration as compared with the inside thereof.

[Claim 45] The spacer according to any one of claims 30 to 44, wherein said highly resistive film is formed by any one of the following methods: sputtering, vacuum deposition, wet printing, spraying, or dipping.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Utilization]

The present invention relates to an electron beam apparatus, an image producer as an application thereof such as an image display and the like, and a spacer for use in the image producer and the like, especially relates to the electron beam apparatus and the image

producer having an atmospheric-pressure resistant structure as well as the spacer for use therein.

[0002]

[Prior Art]

There are two types of electron emission devices currently known: a hot cathode device and a cold cathode device. As to the latter, the known devices include, for example, surface conduction electron emission devices, field emission devices (hereinafter referred to as an FE type) and metal-insulating layer-metal type electron emission devices (hereinafter referred to as an MIM type).

[0003]

The surface conduction electron emission devices currently known include, for example, one disclosed by M. I. Elinson in Radio Eng. Electron Phys., 10, 1290, (1965), and the others described below.

[0004]

The surface conduction electron emission devices take advantage of the phenomenon that electron emission occurs on the thin film of a small area formed on the substrate when applying electric current parallel to the surface of the film. There are several types of surface conduction electron emission devices reported, in addition to the aforesaid device by Elinson et al. which utilizes SnO_2 thin film: one utilizing Au thin film (refer to G. Dittmer: "Thin Solid Films," 9, 317

(1972)), one utilizing In_2O_3/SnO_2 thin film (refer to M. Hartwell and C. G. Fonstad: "IEEE Trans. ED Conf.," 519 (1975)), and one utilizing carbon thin film (refer to Hisashi Araki et al. "Vacuum," Vol. 26, No. 1, 22 (1983)).

[0005]

Fig. 33 shows a plan view of the aforementioned device by M. Hartwell et al. as a typical example illustrating the construction of the surface conduction electron emission devices. In the figure, reference numeral 3001 designates a substrate and numeral 3004 designates a conductive thin film consisting of metal oxide and formed by sputtering. The conductive thin film 3004 is in the form of an H-shaped plan as shown in the figure. An electron emission portion 3005 is formed by conducting an energization treatment, known as energization forming which is to be described below, to the above conductive thin film 3004. The spacings L and W in the figure are set for 0.5 to 1 [mm] and 0.1 [mm], respectively. For convenience's sake, in the above figure the electron emission portion 3005 is shown in the center of the conductive thin film 3004 in the form of a rectangle. The figure is, however, very schematic and does not necessarily represent the actual position and form of the electron emission portion.

[0006]

In the aforesaid surface conduction electron

emission devices, including one by M. Hartwell, it has been common that the electron emission portion 3005 is formed by conducting an energization treatment, called energization forming, to the conductive thin film 3004 prior to the execution of electron emission. Energization forming used herein means that a constant direct-current voltage or a direct-current voltage stepping up at a very slow rate of, for example, about 1 V/min is applied to both ends of the conductive thin film 3004 to pass a current therethrough and cause a local fracture, deformation or change in quality therein, so as to form the electron emission portion 3005 in a highly resistive state. In some part of the conductive thin film 3004 having undergone a local fracture, deformation or change in quality, a crack is to appear. When applying a proper voltage to the conductive thin film 3004 after the above energization forming, electric emission occurs in the vicinity of the above crack.

[0007]

The known FE type devices include, for example, one disclosed by W. P. Dyke & W. W. Dolan in "Field Emission," Advance in Electron Physics, 8, 89 (1956) and one disclosed by C. A. Spindt in "Physical Properties of Thin-Film Field Emission Cathodes with Molybdenium cones," J. Appl. Phys., 47, 5248 (1976).

[0008]

Fig. 34 shows a sectional view of the aforementioned device by C. A. Spindt et al. as a typical example illustrating the configuration of FE type devices. In the figure, reference numeral 3010 designates a substrate, numeral 3011 an emitter wiring consisting of a conductive material, numeral 3012 an emitter cone, numeral 3013 an insulating layer and numeral 3014 a gate electrode. In this device, field emission is caused at the tip portion of the emitter cone 3012 by applying a proper voltage between the emitter cone 3012 and the gate electrode 3014.

[0009]

There is another example of the construction of FE type devices where, unlike the laminated structure shown in Fig. 34, an emitter and a gate electrode are arranged on the substrate almost parallel to the substrate plane.

[0010]

The known MIM type devices include, for example, one disclosed by C. A. Mead in "Operation of Tunnel-Emission Devices," J. Appl. Phys., 32, 646 (1961). Fig. 35 shows a typical example of the construction of MIM type devices. The figure is a sectional view, in which reference numeral 3020 designates a substrate, numeral 3021 a lower electrode consisting of metal, numeral 3022 a thin insulating layer about 100 Å thick and numeral 3023 an upper electrode about 80 to 300 Å thick

consisting of metal. In MIM type devices, electron emission is caused on the surface of the upper electrode 3023 by applying a proper voltage between the upper electrode 3023 and the lower electrode 3021.

[0011]

The aforementioned cold cathode devices do not need a heater for heating their cathode since they allow electron emission to occur at a lower temperature than hot cathode devices. Accordingly, their structure can be simpler than that of hot cathode devices, which allows fine devices to be produced. Further, when multiple devices are densely arranged, problems such as melting substrate by heat and the like are unlikely to occur. In addition, unlike the hot cathode devices, which are slow at response because they operate only after heated with a heater, the cold cathode devices have the advantage of being quick at response.

[0012]

Thus, a lot of studies have been conducted for the application of cold cathode devices.

[0013]

A surface conduction electron emission device, for example, has a particularly simple structure and is easy to produce compared with the other cold cathode devices, accordingly the application of this type devices is advantageous to forming multiple devices over a large area of the substrate. Therefore, methods

have been studied to arrange and drive multiple devices on the substrate, as disclosed, for example, by the present applicants in Japanese Patent Application Laid-Open No. 64-31332.

[0014]

As to the application of surface conduction electron emission devices, the studies have been carried out of, for example, image producer such as an image display and an image recorder, charged beam sources and the like. For the application to an image display, the display using surface conduction electron emission devices in combination with a fluorescent substance, which emits light when electron beam is applied, has been studied as disclosed by the present applicants in U.S. Patent No. 5,066,883, Japanese Patent Application Laid-Open No. 2-257551 and Japanese Patent Application Laid-Open No. 4-28137. An image display using surface conduction electron emission devices in combination with a fluorescent substance is expected to have properties superior to conventional ones using other methods. The above display may be superior to, for example, the liquid crystal display which has been in common use recently in that it does not need a backlight since it spontaneously emits light and in that it has a wide viewing angle.

[0015]

A method for arranging and driving multiple FE

type devices is disclosed, for example, by the present applicants in U.S. Patent No. 4,904,895. The known examples of the application of FE type devices to an image display include, for example, a planar image display reported by R. Meyer et al. (refer to R. Meyer: "Recent Development on Micro-Tips Display at LETI," Tech. Digest of 4th Int. Vacuum Microelectronics Conf., Nagahama, pp. 6-9 (1991)).

[0016]

An example of the application of multiple MIM type devices in the arranged state to an image display is disclosed by the present applicants in Japanese Patent Application Laid-Open No. 3-55738.

[0017]

Among the image producer using the electron emission devices described above, a planar image display which is thin depthwise has attracted considerable attention as a replacement of the image displays utilizing cathode-ray tubes, since it is space-saving and lightweight.

[0018]

Fig. 36 is a perspective view of one example of the display panel constituting a planar image display, partially broken away to show the inside structure.

[0019]

In the figure, reference numeral 3115 designates rear plate, numeral 3116 a side wall and numeral 3117 a

face plate. And the rear plate 3115, the side wall 3116 and the face plate 3117 make up an outer enclosure (hermetic container) for keeping the inside of the panel cell vacuum. On the rear plate 3115 a substrate 3111 is fixed, while on the substrate 3111 N × M cold cathode devices are formed (wherein N, M are positive integers not lower than 2 and they are properly set according to the number of pixels to be displayed). The above N × M cold cathode devices 3112 are wired with M lines of row wiring 3113 and N lines of column wiring 3114 as shown in Fig. 27. The portion consisting of the substrate 3111, the cold cathode devices 3112, the row wiring 3113 and the column wiring 3114 is referred to as a multiple electron beam source. Between the row wiring 3113 and the column wiring 3114 an insulating layer (not shown in the figure) is formed at least at each portion where the row wiring intersects the column wiring. As a result, the row wiring 3113 and the column wiring 3114 can be kept electrically separated from each other.

[0020]

On the underside of the face plate 3117, a fluorescent film 3118 is formed which consists of fluorescent substances of three primary colors: red (R), green (G) and blue (B) (not shown in the figure). Between adjacent fluorescent substances each of which is colored in any one of the above primary colors and

constitutes the fluorescent film 3118, a black substance (not shown in the figure) is provided. And on the surface of the fluorescent film 3118 which faces the rear plate 3115, a metal back 3119 consisting of Al and etc. is formed.

[0021]

Dx1 to Dxm, Dy1 to Dyn and Hv are electrical connection terminals having a hermetic structure for electrically connecting the above display panel with an electric circuit, which does not appear in the figure. Dx1 to Dxm, Dy1 to Dyn and Hv are electrically connected with the raw wiring 3113 of the multiple electron beam source, the column wiring 3114 of the multiple electron beam source and the metal back 3119, respectively.

[0022]

The interior of the above hermetic container is kept at a vacuum of about 10^{-6} Torr. As the display area of the image display becomes larger, some means becomes necessary to prevent the rear plate 3115 and the face plate 3117 from undergoing deformation or fracture due to the difference in atmospheric pressure between the interior and the exterior of the hermetic container. The use of the method in which the rear plate 3115 and the face plate 3117 are made thicker not only increases weight of the image display, but causes distortion of images as well as parallax when viewing

the display at an angle. Contrary to this, in Fig. 36 are provided structural supports (referred to as spacer or rib) 3120 made of a relatively thin glass plate for supporting atmospheric pressure. The spacing between the substrate 3111, which has a multiple electron beam source formed on it, and the face plate 3117, which has a fluorescent film 3118 formed on it, is usually kept submillimeter to several millimeters, and the interior of the hermetic container is kept at a high vacuum as described above.

[0023]

When applying voltage to each cold cathode device 3112 in an image display with the display panel described above through the terminals, Dx1 to Dxm and Dy1 to Dyn, outside the container, electrons are emitted from each cold cathode device 3112. At the same time, a high voltage of several hundreds-volt to several-kilovolt is applied to the metal back 3119 through the terminal Hv outside the container to accelerate the emitted electrons above and force them to collide with the internal surface of the face plate 3117. This allows each colored fluorescent substance constituting the fluorescent film 3118 to be excited and emit light, as a result of which images are displayed.

[0024]

[Problem to be Solved by the Invention]

surface of the spacers by forming a highly resistant thin film as an antistatic film thereon. The antistatic film used in the above patent is a thin film of tin oxide, a mixed crystal thin film of tin oxide and indium oxide, or a metal thin film.

[0027]

The use of the method in which electrical charge is neutralized with a highly resistant thin film sometimes leaves the problem of insufficient reduction of image distortion unsolved. The principal factor underlying this problem is considered to be the concentration of electrical charge in the vicinity of the junction portion due to the insufficient electrical junction between the spacers with a highly resistant thin film and the upper and lower substrates, that is, the face plate (hereinafter referred to as "FP") and the rear plate (hereinafter referred to as "RP"). In order to solve this problem, there is proposed a method in which the end faces of the spacer facing FP and RP, respectively, are coated with the material whose resistivity is lower than a metal thin film or a highly resistive film within the range of about 100 to 1000 micron so as to ensure its electrical contact with the upper and lower substrates and control its electrification due to the incidence of the reflected electrons (emitted electrons) from the face plate, as disclosed in Japanese Patent Application Laid-Open No.

8-180821 and Japanese Patent Application Laid-Open No. 10-144203.

[0028]

Even with such a means given to the highly resistive film and the means for controlling the orbit of emitted electrons, as well as with the formation of low resistive film portion for a better electrical contact as described below, electrification of the spacers cannot be sufficiently controlled depending on the other design parameters of the electron beam apparatus, such as materials and film thickness of its face plate, shape, and anode accelerating voltage, and there still exist problems of, for example, displacement of light emitting points and occurrence of an infinitesimal discharge in the vicinity of the spacers due to the insufficient control.

[0029]

The cause of such electrification is not clarified in detail, it is, however, considered that the factors lie upon the following background.

[0030]

Presumably, the cause of electrification of the spacers is such that there may exist some factors which effectively increase the capacitance and resistance of the spacers as described below, or the spacers are exposed to the reflected electrons from the cold cathode devices 3112 close thereto other than the most

closest ones during their non-selective period and also exposed to the abnormal field emission from the field concentration region in the vicinity of the spacer-cathode junction. In addition, it is considered to be another cause of the electrification that control of the secondary emission coefficient on the surface of the spacers is not accounted for in design.

[0031]

[Background 1] Restriction by the relaxation time constant of a highly resistive film on spacers

The progress of electrification and relaxation in any region of the surface of a spacer can be considered as a time delay of the charged electric potential corresponding to the injection current by the application of a charged dielectric model.

[0032]

Fig. 12 illustrates a model which represents the relaxation by capacitance resistant devices in the case of looking at upper and lower electrodes from a current injection region, when an effective injection current ic is supplied from a current source to an arbitrary position z on the surface of a spacer. In the figure, Va designates a voltage applied from a voltage source to an anode and ic an effective injection current supplied to the position at a height of zh (wherein h corresponds to the height of a spacer, $0 < z < 1$). The effective injection current corresponds to the

difference between a secondary current and a primary current. C1 and R1 designate values of capacitance and resistance, respectively, which specify the relaxation time constant between the injection region and the anode, while C2 and R2 values of capacitance and resistance, respectively, which specify the relaxation time constant between the injection region and the cathode. When the resistance and the capacitance distribute uniformly in the altitude direction, C1, C2, R1 and R2 are described using the resistance of the spacer R and the capacitance C by C/(1 - z), R(1 - z), C/z and Rz, respectively.

[0033]

Since the principle of superposition should hold for the injection current in any position, the electric potential in the region of an arbitrary altitude on the spacer can be specified without losing generality if considering the electrification process in the following manner; first a high voltage Va from a voltage source is applied between the anode and the cathode, then the electronic current entering from the vacuum side to the position z in the aimed region is treated as an effective injection current Ic which is equivalent to the difference between the entered and emitted currents, and finally performing formularization with an equivalent circuit to which the effective injection current Ic as a current source is

supplied, as shown in Fig. 12.

[0034]

Now, in order to design a suitable spacer construction, formularization of a relaxation process will be performed taking a concrete example of the charged electric potential on the spacer having an insulating or highly resistive film formed on it and suitable for the electron beam emission apparatus of the present invention. For simplification, it is assumed that distribution of electric constant is uniform on the surface of the spacer. First, formularization is performed treating the rate of effective injection charge to the surface of the spacer as amount of current supplied from a current source and taking into account the energy distribution and incident angle distribution of incident electrons. The result is as follows:

amount of electronic current emitted from the electron emission device Ie

proportion of the incident electrons at an altitude of zh ($0 < z < 1$) β^{ij}

secondary electron emission coefficient at an altitude of zh ($0 < z < 1$) δ^{ij}

provided that superscripts i, j correspond to incident energy and incident angle, respectively,

amount of primary electronic current in the position z Ip

$$Ip = \Sigma\Sigma Ip^{ij} = \Sigma\Sigma\beta^{ij} \times Ie$$

amount of secondary electronic current in the position z Is

$$Is = \Sigma\Sigma\delta^{ij} \times Ip^{ij} = \Sigma\Sigma\delta^{ij} \times \beta^{ij} \times Ie$$

injection rate of the electrical charge in the position z Ic

$$Ic = \Sigma\Sigma(\delta^{ij} - 1) \times Ip^{ij} = \Sigma\Sigma(\delta^{ij} - 1) \times \beta^{ij} \times Ie$$

[0035]

Finally, the rate of injection charge Ic can be described as

[0036]

[Numerical Formula 5]

$$I_c = P \times I_e \qquad \text{General Formula (2)}$$

[0037]

wherein P is described as $P = \Sigma\Sigma\ (\delta^{ij} - 1) \times \beta^{ij}$ and is a coefficient independent of Ie, it is, however, assumed that in reality P changes as the progress of electrification.

[0038]

Then, for the arrangement of the capacitance and resistance of the spacer film seen from the injection region, it is assumed for simplification that there exists neither resistance variation nor capacitance variation in the altitudinal direction of the spacer (this corresponds to the direction in which a high voltage is applied between anode and cathode). At this time, when the resistance and capacitance in the

direction parallel to the surface of the spacer seen from anode/cathode are represented by R and C, the altitude of the spacer h, and the altitude of the injection region zh ($0 \leq z \leq 1$, on the anode side $z = 1$), the electric constant existing above and below the injection region is specified for the position z. Further, since a voltage from the voltage source is applied between the anode and the cathode, an effective impedance Z is dealt with as 0. Thus, it is understood that the injected electrical charge undergoes relaxation through the parallel resistance and the parallel capacitance of each resistance and capacitance lying above and below the injection region. The resistance and the capacitance between the injection region in the position z and GND are described by $z(1-z)R$ and $C/z + C/(1-z)$, respectively, and response time constant τ of the relaxation path corresponds to the product of the master resistance and capacitance of the spacer, that is, CR at an arbitrary position.

[0039]

The electric potential in any position at this time is described as a function of time using the solution obtained by setting up a differential equation concerning a current for the entire close of the aforementioned equivalent circuit shown in Fig. 12.

[0040]

When the time of starting electron emission is

shown by $t = 0$, provided that electron emission device is continuously driven, $\Delta V(t)$ which represents the progress of charged electric potential in the injection region is described by the following equation,

[0041]

[Numerical Formula 6]

$$\Delta V(t) = z(1-z)Ri_c(1-\exp(-t/\tau)) \quad \text{General Formula (3)}$$

and it is clear that the progress of charged electric potential depends on the product of the resistance R and effective injection current Ic.

[0042]

When plotting time in abscissa and the amount of the emission current from electron emission device and the time of emitting the charged electric potential electrons on the spacer in ordinate, setting quiescent time (that is, selective period, non-selective period) for t1 seconds, and repeating the drive of the device every t2 seconds, as shown in Fig. 5, the charged electric potential ΔV at the end of the first period (t1 + t2 seconds) is described using the general formula (3) as follows:

[0043]

[Numerical Formula 7]

$$\Delta V(t) = z(1-z)Ri_c(1-\exp(-t_1/\tau))\exp(-t_2/\tau) \quad \text{General Formula (4)}$$

And it is assumed that electrical charge is accumulated every time the devices close to the spacer are driven,

provided that t2 >> τ or t1 << τ does not hold. The relaxation process of electrification of the spacer is thus described.

[0044]

On the other hand, the change in the position of a beam with the amount of electrons emitted during the selective period t1 (Duty dependency) is a problem for a display device, however such Duty dependency in the light emitting position can be dealt with as a change of ΔV shown by the general formula (3) corresponding to the amount of emitted electrons (the product of Ie and pulse width), accordingly both sides of the general formula (3) are differentiated by the amount of emitted electrons (the product of Ie and pulse width).

[0045]

[Numerical Formula 8]

$$\frac{d\Delta V(t)}{d(I_e t_1)} = z(1-z)R\left\{\frac{P(1-\exp(-t_1/\tau))}{t1} + \frac{P\exp(-t_1/\tau)}{\tau}\right\}$$
$$= \frac{z(1-z)}{C}\frac{P}{t_1}\{\tau + (t_1-\tau)\exp(-t_1/\tau)\}$$

General Formula (5)

The general formula (5) is simplified by the driving conditions and the material constant. When the material is insulating or selective period is very short, CR = τ >> t1 holds, and the following formula is established.

[0046]

[Numerical Formula 9]

$$\frac{d\Delta V(t)}{d(I_e t_1)} = \frac{z(1-z)P}{C}$$ General Formula (6)

When the material is low resistant or selective period is very long, CR = τ << t1 holds, and the following formula is established.

[0047]

[Numerical Formula 10]

$$\frac{d\Delta V(t)}{d(I_e t_1)} = \frac{z(1-z)PR}{C}$$ General Formula (7)

Now parameters specifying Duty dependency in the light emitting position, that is, tone dependency during the selective period will be explained based on the above formularization.

[0048]

In terms of the conditions under which an accelerating voltage between anode and cathode is maintained, preferably a spacer has some degree of insulating property or high resistance in the direction parallel to its surface. Accordingly, when taking into account Duty dependency of charged electric potential in any position, preferably the general formula (6) is applied. Thus, in order to control Duty dependency, dielectric constant or the section area of the spacer material needs to be enlarged. The controllable range of dielectric constant in material is, however, extremely limited compared with specific resistance, and as for film thickness, it is impossible to ensure an effective dimension for the reason related to

processes. Thus, control of parameter P is required.

[0049]

Further, in terms of the increase in effect of electrification relaxation during quiescent time, if electrons are injected into a spacer in a repetition period shorter than the time constant specified by resistance and capacitance, charges are accumulated, as described with respect to the above general formula (4). Even when the material is applied to the highly resistive film on the surface of the spacer whose relaxation time constant is smaller than the line non-selective period of electron emission device t2 second (≅ selective period × the number of scanning lines), cumulative charge can be formed. Thus the design of relaxation time τ aiming at control of the resistance alone is considered to be insufficient for antistatic measures.

[0050]

In any case, it is difficult to design suitable conditions under which electrification is restricted as long as control of resistance and capacitance alone is aimed at, for this purpose, the control of secondary electron emission coefficient is required.

[0051]

[Background 2] Generally secondary electron emission coefficient largely depends on the incident angle of incident electrons, and secondary electron

emission coefficient δ doubles almost exponentially by enlarging the incident angle.

Generally, in cases where primary electrons enter the smooth surface as shown in Fig. 14, when the incident angle is represented by θ [degree] ($-90 < \theta < 90$), incident energy by Ep [keV], the distance incident electrons penetrate into the film by d [Å], absorption coefficient of secondary by α [1/Å], the mean energy of primary electrons needed for the generation of secondary electrons in the film by ξ [eV] and the probability of secondary electrons escaping from the surface to vacuum by B, secondary electron emission coefficient is quantitatively described using parameters A, n describing the energy loss process of primary electrons in the film by the following general formula (0).

[0052]

[Numerical Formula 11]

$$\delta_\theta = \frac{B}{U}\left(\frac{An}{\alpha}\right)^{\frac{1}{n}}(\alpha d\cos\theta)^{\frac{1}{n}-1}\{1-\exp(-\alpha d\cos\theta)\}$$

General Formula (0)

wherein the penetration distance and incident energy are related by $d = (1/An)\ (E_p)^n$.

[0053]

Here, the incident angle dependency standardized in the general formula (0) for the vertical incidence of 0 degree, that is, θ = 0 can be an index for

evaluating the secondary electron emission multiplication effect at an angle. This is shown below as a general formula (1).

[0054]

[Numerical Formula 12]

$$\frac{\delta_\theta}{\delta_0} = \frac{1}{\cos\theta}\frac{1-\exp(-m_0\cos\theta)}{1-\exp(-m_0)} \qquad \text{General Formula (1)}$$

wherein m_0 is equal to and which is the product of the absorption coefficient of secondary electrons α and the penetration distance of primary electrons d, is a function of incident energy, and can be a positive real number. Hereinafter m_0 is referred to as incident angle multiplication coefficient of secondary electron emission coefficient, because of its characteristics. In the above general formula (1), m_0 shows a tendency to increase monotonously with the incident angle $|\theta|$ under arbitrary incident energy conditions, then rapidly increases where the incident angle becomes about 90 degrees. This is because the primary electrons enter the surface at an angle and the distribution of the secondary electron generating sites shifts near to the surface of the film. For this reason, the proportion of the electrons increases which are emitted into vacuum without recombining and therefore vanishing. This can be understood as an apparent reduction of the absorption coefficient of secondary electrons α to $\alpha\cos\theta$. In the smooth material formed on the smooth surface as an actual spacer

material, for example, an incident angle multiplication coefficient of secondary electron emission coefficient m_0 is larger than 10, provided that the incident energy is 1 keV. Under this condition, the incident angle multiplication coefficient of secondary electron emission coefficient is almost 10 and this is the big cause of the positive electrification of the spacer material. The enlarged incident angle multiplication effect of secondary electron emission coefficient is shown in Fig. 15.

[0055]

[Background 3] The distribution of the incident angle to a spacer is large, in addition, the incident electrons entering the surface at a large incident angle are predominant.

There exist various routes for the electrons' incidence, they are, however, represented roughly by three particular routes. The first one is a direct incidence of the electrons emitted from electron emission devices. In this case, the incident angle is as large as about 80 to 86 degrees, though it depends on the degree of distortion in the electric field near the spacer and other designed values of the apparatus, and its incident mode is a large incident angle and high incident energy. Further, it has a feature such that, since the distance between the spacer and electron emission device close thereto is short, the

amount of incident electrons is very large. The second one is an indirect incidence of the electrons reflected from a face plate to its surroundings. In this route, the distribution of the incident angle expands from 0 to large degrees, and the incident energy also has a distribution, but its range is smaller than that of the incident energy in the first route. The third one is re-incidence to the surface of the spacer of the incident electrons of the first and the second routes or the electrons emitted from field concentration points. This route is considered to occur because electrons are apt to re-enter the region in the locally positively charged state compared to other regions. In this case also, the incident angle has a distribution. Since a high electric field of about several kV/cm to several tens kV/cm is usually applied in the creeping direction as an accelerating voltage, the vertical incidence of electrons is modulated to an incidence at a large angle. Thus, incident electrons passing through any route have an incident angle distribution, and an effective charge injection is performed through the positive charge formed inside of a solid by the incident electrons entering at a large angle. Of the incident modes described above, the direct incident electrons of the first route is usually predominant over the positive charge in question, they are, however, dependent on the driving state and the design of

electron emission device, and they can sometimes leave the problem unsolved of the emitted electrons from a face plate and the re-incidence of multiple scattered electrons described below.

[0056]

[Background 4] Multiple electron emission on the surface

The secondary electrons once emitted from the surface of a spacer have a relatively small initial energy of at most 50 eV. Although in space they receive energy from the electric field between the anode and cathode, since situations in which the spacer is charged positively often occur, there exist many electrons plunging into the positively charged region on the spacer as well as the electrons reaching the anode. These electrons are problematic because they accumulate the positive charge on the spacer cumulatively while repeating their incidence at a low incident energy and a large incident angle and emission alternately. Thus, control of the above multiple electron emission is the subject for study.

[0057]

Now the above backgrounds will be abstracted. As apparent from Background 1, there are some cases where the film designed taking into account resistant value alone is not perfect since the range within which the dielectric constant and resistant value of the film can

be selected is restricted, and in such a case it is important to restrict the amount of effective current injected into the film, or to restrict secondary electron emission coefficient.

[0058]

As apparent from Backgrounds 2 and 3, in the design of the spacer's surface the reduction of incident angle dependency of secondary electron emission coefficient and the absolute value thereof is a subject, since electrification by the electrons with a large incident angle is predominant over the real electron emission devices. Further, Background 4 shows that it is important to reduce the cumulative emission phenomenon of electrons to control the cumulative positive accumulation of multiple scattered electrons. These are the subjects of the art of the present invention.

[0059]

The objects of the present invention are to overcome the above-mentioned subjects, to provide a spacer, which controls electrification by overcoming the subjects described above, and to provide an electron beam apparatus with high definition and long-term reliability in which displacement of emission points and creeping discharge both involved with static electricity are restricted.

[0060]

[Means for Solving the Problem]

Empirically, the above formulae (0) and (1) are satisfied in almost all the materials, and the incident angle multiplication coefficient of secondary electron emission coefficient m_0 is obtained by fitting experimental values in the general formula (1). m_0 can be used as an index of incident angle dependency of secondary electron emission coefficient since it is highly reproductive.

[0061]

According to the present inventors' detailed examination, many inorganic materials having a low secondary electron emission coefficient which have been considered to be suitable for spacers show a strong incident angle dependency and have an incident angle multiplication coefficient of secondary electron emission coefficient m_0 of 10 or larger. This is a significant cause of positive electrification of spacers within image displays of the electron beam emission type where many electrons enter the surface of the spacer at an angle.

[0062]

[Ideal State derived from Theoretical Equation]

What should be done to reduce incident angle multiplication coefficient of secondary electron emission coefficient m_0 as well as to reduce secondary electron emission coefficient δ0 for the vertical

incidence? After the present inventors' detailed examination, it was found that the above subject can be accomplished by satisfying the following requirements. Specifically, it is considered that the methods grouped into two major categories can be used in order to relax incident angle dependency.

[0063]

Those are the methods for relaxing the uniformity of incident angle itself and for reducing surface effect as a property on material side, that is, the ratio of penetration depth of primary electrons to penetration depth of secondary electrons: d/λ.

[0064]

(1) Dispersion of Incident Angle of Primary Electrons

Incident angle is allowed to have an infinitesimal distribution in the normal direction on the interface considered as a surface, so that it is not restricted to the angle specified by the outside. Thus the incident angle defined on a local basis has a distribution with respect to the angle defined on a broader basis, which allows dependency on incident angle to be relaxed. Since dependency on incident angle shows the property of rapidly increasing when incident angle is close to 90 degrees, relaxation by the dispersion of incident angle is significantly effective.

[0065]

(2) Reduction of the Ratio of Penetration Depth of Primary Electrons to Penetration Depth of Secondary Electrons

Since the penetration depth of electrons into a solid is proportional to the reciprocal of free electron density $\rho Z_{eff}/A_{eff}$, a larger free electron density makes possible a smaller incident angle multiplication coefficient of secondary electron emission coefficient m_0. In the devices other than hydrogen, values of Z_{eff}/A_{eff} are in the range of 2 to 2.5, and since its variation is smaller than that of ρ, the penetration depth is specified by the specific gravity ρ of each solid. In other words, when primary electrons have an equal incident energy, their penetration depth becomes smaller in the film having a larger density ρ. Then, since $m_0 = d/\lambda$ (wherein λ is escape depth of secondary electrons, $\lambda = 1/\alpha$), the restriction of incident angle multiplication coefficient of secondary electron emission coefficient m_0 is understood as the restriction of the ratio of penetration depth of primary electrons to penetration depth of secondary electrons within the medium.

[0066]

In a uniform single material system, however, it is very difficult to control the relationship between λ and d independently. After the present inventors'

examination, it was found that incident angle multiplication coefficient of secondary electron emission coefficient m_0 often has a value of 10 or larger.

[0067]

After the present inventors' detailed examination, it was found that the following structures satisfy the requirements for the construction in which the above processes (1) and (2) are performed.

[0068]

According to the result of the present inventor's examination, the escape depth of secondary electrons λ is made to disperse and increase depthwise by constructing the surface of the spacer in such a manner that the incident angle of primary electrons have a distribution in the direction of film thickness. Because of $\lambda \ll d$ in many regions within a solid from the difference between the energies of electrons, the increasing rate of d with the dispersion of incident angle in the surface position is infinitesimal compared with the increasing rate of λ, as a result, d/λ value becomes small and incident angle multiplication coefficient of secondary electron emission coefficient m_0 is reduced. The above method in which incident angle is allowed to have a distribution in the direction of film thickness on the surface of the spacer is implemented by giving the surface of the

spacer a network structure in which multiple localized parts are depressed and arranged in a intricate manner.

[0069]

Increase in λ was attempted with these methods, and it is found that the application of a suitable design allows incident angle multiplication coefficient of secondary electron emission coefficient m_0 to be reduced to about 3.

[0070]

The process of reducing incident angle dependency of secondary electron emission using the network structure consisting of an intricate surface described above is understood as follows.

[0071]

Both of the primary and secondary electrons traveling in the highly resistive film portion gradually lose their energy while interacting with the atoms within the medium and repeating collision and scattering. In such a situation, their penetration depth and energy decreasing rate largely depend on the electron density of the medium they pass through. In the medium having a high electron density, since the probability of their scattering is high, their penetration depth becomes small. In addition, since the energy decreasing rate for a certain penetration distance is large, the amount of secondary electrons generated for unit depth increases. Thus, in the

structure having a high electron density, in other words, in the material having a large specific gravity, penetration depth of electrons is smaller and the amount of secondary electrons generated is larger than those in the material having a small specific gravity.

[0072]

When taking into account the behavior of the secondary electrons generated at the interface of the media different in electron density while taking into account the differences in penetration depth and generation amount, it is considered microscopically that a phenomenon occurs that secondary electrons are emitted from the region where electron density is high into the region where electron density is low.

[0073]

In cases where the above interface is formed unevenly and consequently the surface area is increased, electrons traveling in the low electron density region where penetration depth of incident electrons is large reach again its interface with the high electron density region, thus they lose their energy. Charges remain in the film for a certain period of time in the dielectric polarization, they, however, recombine with positive holes and vanish within the film in the end. After all, most of these electrons are not emitted into vacuum, and the amount of secondary electron emission is decreased.

[0074]

In the present invention, a highly resistive film and vacuum are utilized as the two regions different from each other in electron density, and the geometry of the substrate surface of the foundation underlying the above highly resistive film is made uneven to form an intricate interface.

[0075]

Table 1 shows the processes implemented by the claims of the present invention in an arranged manner.

[0076]

[Table 1]

	Top Surface Unevenness	
	Uneven Substrate + Highly Resistive Film	
Interface (example)	Vacuum	Film
Specific Gravity ρ Electron density $\rho A_{eff}/Z_{eff}$	Small 0	Large
Primary Electron Penetration Depth	Large	Small
Secondary Electron Escape Depth λ	Large	Small
Amount of Secondary Electron Generated $dE/dx/\xi$	Small 0	Large

This structure is allowed to have a function of controlling secondary electrons by dealing with the two regions each of which has a different penetration depth due to the difference in electron density, as an interface and if the structure is constructed in such a

manner that an interface of the two regions different in electron density distributes in the film, it can realize the same effects without limiting the material to a specific highly resistive material.

[0077]

Therefore, the objects of the present invention can be achieved by an electron beam apparatus having the following structure.

An electron beam apparatus according to the present invention comprising an electron source having multiple cold cathode devices, an electrode, which controls electrons emitted from the electron source, a target, which irradiates electrons emitted from the electron source, and a spacer installed between the electron source and the electrode; having an uneven geometry at least on a part of the surface of the spacer substrate, wherein for secondary electron emission of the surface of the spacer substrate having the uneven geometry, the incident angle multiplication coefficient of secondary electron emission coefficient m_0 in

[0078]

[Numerical Formula 13]

$$\frac{\delta_\theta}{\delta_0}=\frac{1}{\cos\theta}\frac{1-\exp(-m_0\cos\theta)}{1-\exp(-m_0)} \qquad \text{General Formula (1)}$$

is 10 or less, and more preferably, m_0 is 5 or less.

[0079]

Also, the electron beam apparatus according to the present invention comprising an electron source having multiple cold cathode devices, an electrode, which controls electrons emitted from the electron source, a target, which irradiates electrons emitted from the electron source, and a spacer installed between the electron source and the electrode; having an uneven geometry at least on a part of the surface of the spacer substrate, wherein a highly resistive film is formed thereon and the average thickness of the highly resistive film is smaller than the average amplitude of the substrate unevenness.

[0080]

Furthermore, unevenness is formed not only in vertical direction against the electrical field direction from an anode to a cathode, but also in multiple directions such as horizontal and oblique so that it can relax incident angles.

[0081]

It is also acceptable that in the above-mentioned uneven structure of the spacer, its forming direction, arrangement and cycle of unevenness are distributed in multiple ways, and the uneven structure may have a random distribution as one geometry.

[0082]

Alternatively, the electron beam apparatus comprises the spacer, which has a highly resistive film

on its surface and a conductive film on the contact surface between the electron source and electrode, wherein the highly resistive film is electrically connected to the electron source and electrode via the conductive film.

[0083]

The electron beam apparatus according to the present invention may also have the following geometry.

[0084]

(1) The electron beam apparatus comprises the electrode which is an accelerated electrode for accelerating electrons emitted from the electron source and forms an image producer which produces images by irradiating electrons emitted from the cold cathode device to the target in accordance with an input signal, especially forms an image display in which the target is fluorescent substance.

[0085]

(2) The cold cathode device is a cold cathode device having a conductive film including an electron emission portion between a par of electrodes, and preferably is a surface conduction electron emission device.

[0086]

(3) The electron source is constructed in a simple matrix arrangement having multiple cold cathode devices wired in a matrix with multiple rows of wiring

and multiple columns of wiring.

[0087]

(4) The electron source has an ladder-shaped arrangement wherein multiple rows (called row wiring) of wiring are formed by connecting multiple cold cathode devices in a row to each other at each of their ends are arranged, the electrons from the cold cathode device are controlled by a control electrode (also called grid) arranged over the above cold cathode device along the direction intersecting these multiple rows of wiring (called column wiring).

(5) According to the concept of the present invention, the present invention is applicable not only to an image producer suitable for displaying, but to a light emission source for the alternative to the light emitting diode etc. of an optical printer consisting of a photosensitive drum, light emitting diodes, etc. And the above image producer is applicable not only to a linear light emission source, but to a two-dimensional light emission source if the above m rows of wiring and n columns of wiring are properly selected. In this case, the image producing member is not limited to the substances directly emitting light, such as fluorescent substances used in the embodiments described below, but the member is also applicable on which a latent image is formed due to the charge by electrons. Further, according to the concept of the present invention, the

present invention is applicable to the cases where the member exposed to the electrons from the electron source is other than image producing member such as fluorescent substances, for example, as is the case of electron microscopes. The present invention may be constituted of a general electron beam apparatus which does not specify a member exposed to the electrons.

[0089]

[Embodiment(s)]

The preferred embodiments of the present invention will be described below.

[0090]

The present invention is an uneven substrate having on its surface a highly resistive film for preventing static electricity, and the unevenness on the spacer substrate is formed so that it can relax incident angles in multiple directions. Referring now to the drawings, (b) and (c) of Fig. 1 are schematic sectional views showing an uneven substrate of the spacer embodying the present invention. (b) of Fig. 1 is a section taken on longitudinal line B-B′ in (a) and (c) of Fig. 1 is a section taken on transverse line C-C′ in the same. In the Figure, reference numeral 1 designates a spacer substrate having unevenness formed at least on its surface, numeral 2 a highly resistive film formed on the surface of the spacer substrate 1 for preventing static electricity. The final form of

[0092]

[Functions of Unevenness (incident angle dependency of static electricity due to secondary electron emission)]

[Direction of Unevenness Formation] Multiple directions, Random

Referring to the drawings, Figs. 2 to 9 show the other structures of the spacers in accordance with the present invention whose substrates are uneven and coated with a highly resistive film, and the same figures also illustrate the geometry of a part of their substrate surface. The functions performed by the unevenness formed on the surface of the spacer in accordance with the present invention have multiple effects, for the multiple problems described above in the item of the problems to be solved, as follows.

[0093]

First, the unevenness is effective in decreasing the incident angle of the incident electrons in a high incident angle mode which largely contributes to the amount of the result is obtained that the incident angle multiplication coefficient of secondary electron emission coefficient m_0 defined in the general formula (1) is decreased. In particular, m_0 is restricted to a level of one third or less as high as that of the smooth surface. This is particularly effective against the incident electrons directly from the electron

emission device closest to the spacer whose incident angle is 80 degrees or higher.

[0094]

Second, the forms of uneven geometry include, for example, a porous structure as shown in Fig. 3, such a structure, like an integration of fine Faraday cups, is effective in shutting secondary electrons in the film.

[0095]

In order to confirm the effects of roughing the spacer surface on the restriction of secondary electron emission, observed with a scanning electron microscope were two types of alumina substrates on which a CrAlN film was formed under the same conditions: an alumina substrate whose surface was subjected to roughing (an alumina substrate having a roughed surface layer) and an alumina substrate whose surface was smooth. Fig. 16 shows the micrographs. (a), (b) and (c) of Fig. 16 show the amount of secondary electron emission when the incident angles of primary electron are 0, 30 and 60 degrees, respectively. In this case, the primary electron acceleration voltage was 1 kV, and the surface of the alumina substrate was coated with a highly resistive film of CrAlN whose thickness is 200 nm. The left half of each figure shows an alumina substrate subjected to roughing and the right half a smooth alumina substrate. The larger the amount of secondary electron emission becomes, the lighter the micrograph

becomes. The results show that the amount of secondary electron emission was restricted by roughing the substrate surface, provided the incident angles were large.

[0096]

Third, the unevenness is effective in restricting the multiple emission of secondary electrons. The secondary electrons having been emitted have orbital motion toward the anode while being accelerated by the energy received from an accelerating field. However, the energy is relatively small immediately after the emission, and the above electrons are pulled into the locally charged region and rush to the surface of the spacer again. This causes $(\delta - 1)$-fold positive charge to be generated. In such a situation, subjecting the substrate surface to roughing makes it possible to cut off the track length of the secondary electrons, and the electrons re-enter the surface of the spacer under the conditions that $\delta - 1 \leq 0$ or $\delta - 1 > 0$, but the absolute value $|\delta - 1|$ is not so large. This is effective in restricting the accumulation of positive charges.

[0097]

Fourth, the highly resistive film in accordance with the present invention is effective in restricting the incident angle of the electrons reflected from the anode.

[0098]

The flying route of the incident electrons into the spacer has various distributions. In cases where the electrons emitted from the face plate re-enter the spacer (hereinafter referred to as FP emitted electrons), the emission direction has a distribution almost in the form of a concentric circle, accordingly the emitted electrons have a distribution in many directions in the circumstances.

[0099]

After the present inventors' intensive examination of the spacer-electron emission device distance dependency and the anode (anode substrate provided on the face plate) voltage dependency of the static electricity of each spacer with respect to the distribution of FP reflected orbit observed from the high voltage application side when driving the electron emission devices row by row, it has been found that the electrons emitted from the anode substrate (the metal back or the anode electrode provided on the face plate) includes not only the electrons emitted from the closest electron emission device (the first closest), but the electrons from the second, third and fourth closest electron emission devices. The effects of the above track length vary depending on the image display because each image display is differently modulated, the effects are, however, doubled by the installation

of the members, such as an aluminium electrode which is provided to promote efficiency in utilizing the light emitted from fluorescent substances, and by the increase in acceleration voltage applied, the above installation and the increase in voltage are generally carried out for the purpose of obtaining a high luminance, though. This is one of the causes for the static electricity on the spacer. The above phenomenon means that FP reflected electrons are dependent on the distance of the electron reflecting position of the face plate from the spacer and that the amount of the electrons re-entering is larger at the device closer to the spacer. In addition, the phenomenon means that, among the FP reflected electrons, the ones reflected in the position closer to the spacer have their incident angles more doubled when re-entering the point far away from the reflecting position. For these reasons, the unevenness formed in multiple directions effectively functions for restricting the secondary electron emission with respect to the reflected electrons in a angled mode.

[0100]

The main functions of roughing the substrate surface or of an uneven substrate surface have been described above in terms of the restriction of static electricity in the present invention. The unevenness, however, produces another effect such that the surface

geometry within the spacer substrate can be easily controlled, as the unevenness is provided on the spacer substrate and its functions are separated from those of the antistatic film.

[0101]

[Cyclicity of Unevenness]

In the electron beam apparatus in accordance with the present invention, the arrangement of the unevenness on the spacer is not necessarily limited to one cyclic arrangement even in order to obtain the effects on restricting the secondary electron emission, random cyclic arrangements are also acceptable. The arrangement may be determined in terms of simplicity and convenience in production process. In cases where the arrangement is cyclic, in particular, the evenness is preferably formed to have a repeating cycle consisting of a multiple cycle structure considering the energy distributions of secondary electrons and reflected electrons as well as the incident angle distribution. The term "multiple cycle structure" used herein means a structure in which multiple cycles are superposed.

[0102]

[Details of Unevenness] Pitch, Amplitude

In terms of the relaxation of the incident angle dependency of secondary electron emission coefficient, the effects of the uneven geometry of the spacer

substrate are not largely dependent on the spacing and the amplitude of the unevenness. And they can be selected arbitrarily. However, considering the effects of trapping the multiply emitted secondary electrons before they obtain an energy from the field in the gap between the anode and cathode and have an acceleration energy for entering the positively charged region, the unevenness of the spacer substrate preferably have a spacing or pitch of about 100 μm, and more preferably 10 μm or shorter. As for the amplitude of the unevenness, its value can be arbitrarily selected in terms of the relaxation of the incident angle dependency of secondary electron emission coefficient for the same reason as above. However, its average roughness is preferably as large as 0.05 μm or more in terms of the restriction of multiply emitted second electrons, and preferably as large as 100 μm or less, which is the upper limit, in terms of the restriction of the field-concentration-effect.

[0103]

[Details of Uneven Geometry] Production Method

The method of producing the above uneven geometry of the spacer is not limited to the one described below. As long as the above geometry can be formed, any method may be selected freely and the combination of multiple methods may be applicable. For example, grating formation method, etching method and lift-off method

are applicable as a technique for microprocessing glass materials. If necessary, the geometry can be controlled using an optical patterning and a mechanical mask.

[0104]

Further, for obtaining a randomly uneven geometry, methods of spraying solid, liquid, particles or the like, such as sand blasting method, may be used. As a method of forming deeply depressed portions, in other words, a porous surface, porous glass and porous ceramic which are produced by subjecting the glass material and the ceramic material consisting of split-phase component to corrosion treatment are applicable. Further, micro-holes obtained electrochemically by subjecting metal surface to anodic oxidation are applicable. These are preferable methods because the density and shape of the porous geometry can be highly controllable by the processing time, heating temperature, the normality of corrosive, the current density etc.

[0105]

Even in cases where the substrate itself does not have an uneven surface, a multilayer type uneven substrate can be used in which an uneven layer is provided between the spacer substrate and the highly resistive surface film. The method of producing an uneven layer is also not limited to the one described

below. However, a film with a roughed surface of a fine-particle dispersion type is preferably used in which fine particles of silicon oxide, metal oxides etc. are dispersed in a binder matrix. Because the above type is characterized in that spacing between the unevenness and the amplitude of the same can be controllable and the unevenness have no sharp projections.

[0106]

For the members relatively easy to melt, such as a glass member, it is possible that first a die is formed from the master which is produced using various surface-roughing means described above, then the substrate is subjected to shape processing using the above die by injection molding, rolling, roll stamping etc.

[0107]

[Resistance Value of Highly Resistive Film (δ of Highly Resistive Film, Construction of Highly Resistive Film)]

In the present invention, basically various types antistatic films can be used as a film on the substrate, as long as they can have unevenness on their surface following the uneven geometry of the underlying layer.

[0108]

In order to form a highly resistive film whose uneven geometry is low in leveling, basically it is

important that the film is formed not to have a significantly large thickness as compared with the desired amplitude of the unevenness of the underlying layer or the substrate. And it is preferable that the film is formed to have a thickness smaller than the amplitude of the underlying layer. However, the extremely thin film means losing the effect on increasing the sheet resistivity as well as losing the continuity of the film in the region where the curvature of the unevenness is large. Thus, when not taking advantage of the conductivity of the substrate, the conditions under which film thickness is at least 100 Å or larger, and preferably 500 Å or larger are selected.

[0109]

As a method of forming a highly resisitive film, the existing processes for forming an antistatic film are applicable. For example, sputtering, vacuum evaporation, wet printing process, spraying process, dipping process and so on are applicable. Liquid phase processes such as dipping process are preferable in terms of lowering costs of production process. In such a process, in order to lower the leveling, it is important to control the film thickness and the viscosity of the coating liquid so that they will be kept small.

[0110]

Further, in highly resistive films, it is preferable that the secondary electron emission coefficient is low. In smooth films, it is more preferable that the secondary electron emission coefficient is 3.5 or lower. In other words, it is preferable that the number of the secondary electrons emitted form the smooth film surface formed on the smooth substrate to the number of the primary electrons entering the same under vertical incident conditions is 3.5 or smaller in all the incident energies. Further, it is preferable in terms of chemical stability of the film that the surface layer of the highly resistive film is in a highly oxidized state as compared with the inside of the film.

[0111]

Referring to Fig. 17, in the image display of the present invention, one side of the above spacer 1020 is electrically connected to the wiring on the substrate 1011 on which cold cathode devices are formed. And the opposite side of the same is electrically connected to the accelerating electrode (metal back 1019) for causing the electrons emitted from the cold cathode devices to collide with the light emitting material (fluorescent film 1018) with a high energy. Specifically, a current whose amount is equivalent to the amount of accelerating voltage divided by the resistance value of the antistatic film flows through

the antistatic film formed on the spacer.

[0112]

Thus, the resistance value Rs of the spacer is set for a value within the range desirable in terms of its antistatoc effect and power consumption. In terms of the antistatic effect, preferably the sheet resistivity R/□ is 10^{12} Ω/□ or lower. In order to obtain a sufficient antistatic effect, it is more preferable that the sheet resistivity R/□ is 10^{11} Ω/□ or lower. Although the sheet resistivity is dependent on the shape of the spacer and the voltage applied between the spacers, preferably it is 10^{5} Ω/□ or higher.

[0113]

As for the thickness of the highly resistive film t, preferably it is in the range of 10 nm to 1 μm. Generally, in the thin films of 10 nm or smaller thickness, they take the form of an island, their resistance is unstable, and they lack reproducibility, although they vary depending on the surface energy of the material and the adhesion to and the temperature of the substrate. On the other hand, in the thin films of 1 μm or larger, their film stress becomes heavier, therefore, there arises a fear of film peeling, and their film formation time becomes longer, therefore, their productivity becomes low. In light of the above points, preferably the thickness of the highly resistive film is in the range of 50 to 500 nm.

[0114]

Considering that the sheet resistivity R/□ is ρ/t and that preferable ranges of R/□ and t are as described above, preferably the specific resistance ρ of the antistatic films is from 10 to 10^8 Ωcm. In order to realize more preferable ranges of sheet resistivity and film thickness, desirably ρ is from 10^2 to 10^6 Ωcm.

[0115]

As described above, the temperature of the spacer rises when current flows through the antistatic film formed thereon or when the entire display generates heat during its operation. If the antistatic film has a temperature coefficient of resistance which is significantly negative, its resistance value decreases with temperature increase, which leads to increase in the current flowing through the spacer, and hence increase in temperature. And the current continues to rise till the power source reaches its limits. Empirically, the values of temperature coefficient of resistance at which such a thermal runaway takes place are negative and their absolute values are 1 % or larger. In other words, it is preferable that the temperature coefficient of resistance of the antistatic film is less than -1 %.

[0116]

As a material having an antistatic film property,

metal oxides are excellent. Among the metal oxides, the oxides of chromium, nickel and copper are preferable materials. The reason is considered to be that their efficiency in emitting secondary electrons is relatively low, accordingly, the spacers are hard to be charged even if the electrons emitted from the electron emission devices collide with them. Among the materials other than metal oxides, carbon is a preferable material because its efficiency in emitting secondary electrons is low. Since amorphous carbon is particularly highly resistive, the use of it makes it easier to control the resistance value of the spacer as desired.

[0117]

However, the above metal oxides and carbon are hard to adjust their resistance value to the specific resistance range desirable for an antistatic film, in addition, their resistance values are easily changed by the atmosphere. Thus these materials alone lack resistance controllability.

[0118]

The nitrides of aluminium-transition metal alloy are suitable materials because their resistance values can be controlled over a wide range from a good conductor to an insulating material by adjusting the composition of the transition metal. In addition, since their resistance values change only a little in

the production process of an image display described below, they are stable materials. Further, since their temperature coefficients of resistance are less than -1 %, they are easy to practically use. The above transition metals include, for example, Ti, Cr and Ta.

[0119]

[Composition Range for obtaining Preferable Specific Resistance]

The antistatic film in accordance with the present invention may be such that a metal oxide film or a carbon film whose secondary electron emission coefficient δ is small is laminated as a top coat layer on a film of aluminium-transition metal alloy nitride (hereinafter referred to as "alloy nitride film" for short). The resistance value of the antistatic film as a whole is almost specified by the resistance value of the alloy nitride film, and the top coat layer functions for restricting the antistatic performance. Since the resistance value of the top coat layer varies depending on the atmosphere, as described above, the thickness of the top coat layer should be determined so that its resistance value will be more than one-half of the resistance value of the antistatic film. However, if the specific resistance of the top coat layer is high, it is difficult to allow the electrons accumulated on its surface to escape; thus, the thickness of the top coat layer is restricted, and

preferably the value is equal to or less than 20 nm.

[0120]

The above alloy nitride film is formed on the insulating member using the thin film formation methods such as sputtering, reactive sputtering in the nitrogen gas atmosphere, electron beam evaporation, ion plating, and ion assist evaporation. The metal oxide films can be also formed using the same thin film formation methods as above, in this case, however, oxygen gas is used instead of nitrogen gas. The other methods, such as CVD and alkoxide application, are also applicable to the formation of the metal oxide films. The carbon film is formed using the methods such as evaporation, sputtering, CVD and plasma CVD, and in cases where amorphous carbon film is formed, the atmosphere is made to contain hydrogen or hydrocarbon gas is used for the deposition gas.

[0121]

The above alloy nitride film and the top coat layer may be formed in separate systems, the adhesion of the top coat layer, however, becomes better when those two are continuously laminated.

[0122]

The antistatic films of the present invention have been described in terms of preventing static electricity of the spacers of a planar image display, their applications are, however, not limited to this,

they can be used as an antistatic film in a different way.

[0123]

The spacer provided with the above highly resistive film is characterized in that it has a low resistive film on the portion in contact with the upper and lower substrates, which makes possible the restriction of the local accumulation of charges in the vicinity of the spacer-anode/cathode junctions. Preferably the resistance value of the low resistive film is 1/10 times or less as high as that of the above highly resistive film and 10^7 [Ω/□] or lower, by sheet resistivity, in order to obtain its satisfactory electrical connection with the upper and lower substrates. In terms of obtaining devices having a simpler structure as well as obtaining a high luminance, the above electron emission devices are more preferably characterized in that they are cold cathode devices, include an electrically conductive film comprising an electron emission portion between the pair of electrodes, and are surface conduction electron emission devices.

[0124]

The electron beam apparatus to which the art of the present invention is applied can be also used as an image producer for producing an image by exposing the aforementioned target to the electrons emitted from the

above electron emission device in response to input signals. In terms of image recording, there are various materials applicable to the above target which make possible the formation of a latent image, however the target consisting of fluorescent substances allows to record and display dynamic images at lower cost.

[0125]

[Rough Summary of Image Display]

The construction of display panels of image displays to which the present invention is applied and the method of producing such panels will be described taking concrete examples.

[0126]

Fig. 17 is a perspective view, partially broken away, showing a display panel used in the embodiments with the internal structure being visualized.

[0127]

In the figure, reference numeral 1015 designates a rear plate, numeral 1016 a side wall, numeral 1017 a face plate, and 1015 to 1017 form a hermetic container for maintaining the inside of the display panel vacuum. When assembling the hermetic container, the junctions of each member need to be sealed so as to maintain a sufficient strength and airtightness. And the sealing was achieved by, for example, coating the junctions with frit glass and firing them at 400 to 500°C in the atmospheric air or in the nitrogen atmosphere for more

than 10 minutes. The method of evacuating the hermetic container will be described below. Since the inside of the above hermetic container is maintained at vacuum of about 10^{-6} [Torr], spacers 1020 as an atmospheric-pressure resistant structure are provided so as to prevent the hermetic container from being fractured by atmospheric pressure or a sudden impact.

[0128]

Then substrates of electron emission devices applicable to the image producer of the present invention will be described.

[0129]

The substrate of an electron source for use in the image producer of the present invention is formed with multiple cold cathode devices arranged on it.

[0130]

There are several ways of arranging cold cathode devices. For example, a ladder arrangement is such that cold cathode devices are arranged in a row and connected to each other at each of their ends through wiring (hereinafter referred to as "ladder arrangement electron source substrate"). And a simple matrix arrangement is such that each pair of device electrodes of cold cathode devices are connected to each other through the wiring in the X direction and wiring in the Y direction (hereinafter referred to as "matrix arrangement electron source substrate"). Image

producers comprising a ladder arrangement electron source substrate need a control electrode (grid electrode) for controlling the flight of the electrons emitted from the electron emission devices.

[0131]

On the rear plate 1015 is fixed a substrate 1011 on which N × M cold cathode devices 1012 are formed (wherein N, M are the positive integers of 2 or more and they are set properly according to the number of the pixel to be displayed. For example, in the image displays for high-definition televisions, desirably N is set for 3000 and M is set for 1000 or more). The above N × M cold cathode devices are wired in a simple matrix with M rows of wiring 1013 and N columns of wiring 1014. The portion consisting of the above 1011 to 1014 is called a multiple electron beam source.

[0132]

For the multiple electron beam sources for use in the image display of the present invention, the material and shape of the cold cathode devices as well as the production method thereof are not restricted at all as long as they are wired in a simple matrix or arranged in a ladder form.

[0133]

Accordingly, cold cathode devices, such as surface conduction electron emission devices, FE type devices and MIM type devices, are applicable.

[0134]

Now the structure of the multiple electron beam source will be described where surface conduction electron emission devices (described below), as cold cathode devices, are arranged in a simple matrix wiring on the substrate.

[0135]

Referring to the drawings, Fig. 17 shows a plan view of the multiple electron beam source used in the display panel of Fig. 20. On the substrate 1011, are arranged the same surface conduction electron emission devices 1012 as shown in Fig. 19 described below which are wired in a simple matrix arrangement with row wiring 1013 and column wiring 1014. On the portion where the row wiring 1013 and the column wiring 1014 intersect, an insulating layer (not shown in the figure) is formed between the electrodes so as to keep them electrically insulating.

[0136]

Fig. 21 is a cross sectional view of the multiple electron beam source of Fig. 20, taken along the line B-B′.

[0137]

The multiple electron beam source having such a structure was produced in such a manner that, first, row wiring 1013, column wiring 1014, an insulating layer between electrodes (not shown in the figure), and

an device electrode and conductive thin film of a surface conduction electron emission devices 1012 were formed on a substrate, then energization forming processing (described below) and energization activation processing (described below) were conducted by feeding power to each device via row wiring 1013, column wiring 1014.

[0138]

The present embodiment has been described taking for example the construction where the substrate of the multiple electron beam source 1011 is fixed on the rear plate 1015 of the hermetic container. However, the substrate of the multiple electron beam source 1011 itself may be used as a rear plate of the hermetic container as long as the substrate 1011 has a sufficient strength.

[0139]

On the rear side of the face plate 1017 is formed a fluorescent film 1018. Since the present embodiment is a color image display, the portion of the fluorescent film 1018 is coated with fluorescent substances of the three primary colors: red, green and blue, which are used in the art of CRT, in a certain pattern. The fluorescent substances of the three different colors are coated on the film, for example, in stripes as shown in (a) of Fig. 22, and between the strips is provided a black conductor 1010. The

purposes of providing the conductor 1010 are, for example, to prevent the occurrence of shear in display color when electron beams a little bit deviate from the right position, to prevent the reflection of external light so as not to decrease the display contrast, and to eliminate the charge-up of the fluorescent film resulting from the exposure to electron beams. Although graphite was used for the black conductor 1010 as a main component, the materials are not limited to this as long as they answer the above purposes.

[0140]

The coating patterns of the three primary colors are not limited to the stripes shown in (a) of Fig. 22, either; a delta pattern and the other patterns (for example, the pattern shown in Fig. 23) are also applicable as shown in (b) of Fig. 22.

[0141]

When producing display panels in monochrome, the fluorescent substance of a single color is used for the fluorescent film 1018 and the black conductor 1010 is not necessarily used.

[0142]

On one side, which is nearer to the rear plate, of the fluorescent film 1018 is provided a metal back 1019, which is well known in the art of CRT. The purposes of providing the metal back 1019 are, for example, to subject part of the light emitted by the fluorescent

film 1018 to its mirror reflection and improve a light usage ratio, to protect the fluorescent film 1018 against the collision with negative ions, to utilize it as an electrode for applying an accelerating voltage to electron beams, and to utilize it as a conductive path for electrons emitted by the fluorescent film 1018 in an excited state. The metal back 1019 was formed in such a manner that, first, a fluorescent film 1018 was formed on the face plate substrate 1017, then the fluorescent film was subjected to smoothing processing, followed by vacuum deposition with Al. When a material for a low voltage is used for the fluorescent film 1018, the metal back 1019 is not necessarily used.

[0143]

Although it was not used in the present embodiment, a transparent electrode made of, for example, ITO may be provided between the face plate substrate 1017 and the fluorescent film 1018 in order to apply an accelerating voltage and to improve the conductivity of the fluorescent film.

[0144]

Fig. 18 is a schematic sectional view of the display panel of Fig. 17, taken along the line A-A', and reference numerals of each portion correspond to those of Fig. 17. The spacer 1020 consists of a member including an insulating member 1, a highly resistive film 11 formed on the surface of the above insulating

member 1 to prevent static electricity, and a low resistive film 21 formed on touching portions 3 facing the inside of the face plate 1017 (metal back 1019 or the like) and the surface of the substrate 1011 (row wiring 1013 or column wiring 1014), respectively, as well as on the side surfaces 5 which is in contact with the above touching portions 3. The necessary number of the spacers are spaced and fixed to the inside of the face plate and the surface of the substrate 1011 via a jointing material 1041. The highly resistive film is formed on the surface of the insulating member 1 at least at the portion exposed to vacuum within the hermetic container, and it is electrically connected to both the inside of the face plate 1017 (metal back 1019 or the like) and the surface of the substrate 1011 (row wiring 1013 or column wiring 1014) via the low resistive film 21 on the spacer 1020 and the jointing material 1041. In the embodiments described here, the shape of the spacer 1020 is in a form of a thin plate, the spacer is arranged in parallel to the row wiring 1013 and is electrically connected thereto.

[0145]

The spacer 1020 needs to have a sufficient insulating property to withstand a high voltage applied between the row wiring 1013/the column wiring 1014 on the substrate 1011 and the metal back 1019 inside of the face plate 1017. At the same time it needs to have

a sufficient conductivity to prevent itself from being charged.

[0146]

The insulating member 1 of the spacer 1020 includes ceramics member, such as quartz glass, glass with impurities such as Na and so on reduced in it, soda-lime glass, and alumina. Preferably the insulating member 1 is such that its thermal expansion coefficient is close to that of the member constituting the hermetic container and the substrate 1011.

[0147]

As mentioned above, it is desirable that the sheet resistivity R/□ of the spacer 1020 is set in the range from 10^5 to 10^{12} Ω/□ from the viewpoints of antistatic electricity and power saving, and it is further desirable to set within the range from 10^5 to 10^{11} Ω/□.

[0148]

Also, as mentioned above, it is preferably to set the thickness of the antistatic film t formed on the insulated material in the range of 10 nm to 1 μm, and it is further preferable being in the range of 50 to 500 nm.

[0149]

Further, as described above, the sheet resistivity R/□ is ρ/t, so it is preferable that the specific resistance ρ of the antistatic films is in the range from 0.1 to 10^8 Ωcm from the preferable ranges of the

sheet resistance and antistatic film mentioned above. It is further preferable to be in the range from 10^2 to 10^6 Ωcm.

[0150]

Furthermore, as mentioned above, it is preferable that the temperature coefficient of resistance of the antistatic film is less than -1 %.

[0151]

As a material for the highly resistive film 11, which has an antistatic property, therefore, is used for an antistatic film as described above, metal oxides, for example, are applicable. Among the metal oxides, the oxides of chromium, nickel and copper are preferable materials. The reason is considered to be that their efficiency in emitting secondary electrons is relatively low, accordingly, the spacers 1020 are hard to be charged even if the electrons emitted from the cold cathode devices 1012 collide with them. Among the materials other than metal oxides, carbon is a preferable material because its efficiency in emitting secondary electrons is low. Since amorphous carbon is particularly highly resistive, the use of it makes it easier to control the resistance value of the spacer as desired.

[0152]

As described above, as another material for the highly resistive film 11, which has an antistatic

property, however, the above metal oxides and carbon are hard to adjust their resistance value to the desired specific resistance range as an antistatic film, in addition, their resistance values are easily changed by the atmosphere. Thus these materials alone lack resistance controllability.

[0153]

As described above, the nitrides of aluminium-transition metal alloy are suitable materials because their resistance values can be controlled over a wide range from a good conductor to an insulating material by adjusting the composition of the transition metal. In addition, since their resistance values change only a little in the production process of an image display described below, they are stable materials. Further, since their temperature coefficients of resistance are less than -1 %, they are easy to practically use. The above transition metals include, for example, Ti, Cr and Ta.

[0154]

As described above, the above alloy nitride film is formed on the insulating member using the thin film formation methods such as sputtering, reactive sputtering in the nitrogen gas atmosphere, electron beam evaporation, ion plating, and ion assist evaporation. The metal oxide film can be also formed using the same thin film formation methods as above, in

this case, however, oxygen gas is used instead of nitrogen gas. The other methods, such as CVD and alkoxide application, are also applicable to the formation of the metal oxide films. The carbon film is formed using the methods such as evaporation, sputtering, CVD and plasma CVD, and in cases where amorphous carbon film is formed, the atmosphere is made to contain hydrogen or hydrocarbon gas is used for the deposition gas.

[0155]

The purpose of providing a low resistive film 21 to the spacer 1020 as a component thereof is to electrically connect the highly resistive film 11 with both of the face plate 1017 (metal back 1019 or the like) having a higher voltage and the substrate 1011 (wiring 1013, 1014 or the like) having a lower voltage. Thus, hereinafter it is sometimes referred to as an intermediate electrode layer (intermediate layer). The intermediate electrode layer (intermediate layer) can have multiple functions listed below.

[0156]

(1) To electrically connect the highly resistive film 11 to the face plate 1017 and the substrate 1011

[0157]

As described above, the highly resistive film 11 is provided to prevent the surface of the spacer 1020 from being charged. However, when the highly resistive

film 11 is connected with both of the face plate 1017 (metal back 1019 or the like) and the substrate 1011 (wiring 1013, 1014 or the like) directly or via the jointing material 1041, a large contact resistance may be generated at the interface of their connection, which may make impossible the prompt elimination of the charges generated on the surface of the spacer 1020. In order to avoid this, the intermediate layer of low resistance is provided on the touching portion 3 of the spacer 1020 which is in contact with the face plate 1017, the substrate 1011 and the jointing material 1041, and the side surface 5 of the spacer 1020.

[0158]

(2) To allow the voltage distribution of the highly resistive film 11 to become uniform

[0159]

The electrons emitted from a cold cathode device 1012 form an electron orbit in accordance with the voltage distribution formed between the face plate 1017 and the substrate 1011. In order to prevent the disorder of the electron orbit from taking place in the vicinity of the spacer 1020, it is necessary to control the voltage distribution of the highly resistive film 11 over the entire region. When the highly resistive film 11 is connected to the face plate 1017 (metal back 1019 or the like) and the substrate 1011 (wiring 1013, 1014 or the like) directly or via the jointing material

1041, non-uniformity occurs in the connecting state due to the generation of contact resistance at the interface of their connection. As a result, it is likely that the voltage distribution of the highly resistive film 11 will deviate from the desired value. In order to avoid this, the intermediate layer of low resistance is provided on the entire length of the end portion of the spacer (touching surface 3 or side surface 5) where the spacer 1020 and both the face plate 1017 and the substrate 1011 abut with each other. The voltage of the highly resistive film 11 can be controlled over the entire region by applying the desired voltage to this intermediate layer.

[0160]

(3) To control the orbit of the emitted electrons

[0161]

The electrons emitted from a cold cathode device 1012 form an electron orbit in accordance with the voltage distribution formed between the face plate 1017 and the substrate 1011. For the electrons emitted from the cold cathode device 1012 in the vicinity of the spacer, restriction involved with the installation of the spacer 1020 (changes in wiring, device position etc.) may occur. In such a case, in order to produce an image free from distortion and non-uniformity, it is necessary to control the orbit of the emitted electrons so that the desired position on the face plate 1017 is

exposed to the electrons. Providing a low resistive intermediate layer on the side surfaces 5 where the spacer and both of the face plate 1017 and the substrate 1011 abut with each other makes possible the realization of a desired property in the voltage distribution in the vicinity of the spacer 1020, which in turn enables the control of the orbit of the emitted electrons.

[0162]

The low resistive film 21 can be selected from the films containing materials whose resistance value is lower than the materials of the highly resistive film 11 by an order of magnitude. The material of the low resistive film 21 is properly selected from the group consisting of metals such as Ni, Cr, Au, Mo, W, Pt, Ti, Al, Cu and Pd or their alloy, printed conductor consisting of metals such as Pd, Ag, Au, RuO_2, Pd-Ag or their oxides and glass etc., a transparent conductor such as In_2O_3-SnO_2, and semiconductor materials such as poly-silicon.

[0163]

The jointing material 1041 needs to have conductivity so that the spacer 1020 can electrically connect to the row wiring 1013 and the metal back 1019. Specifically, frit glass to which a conductive adhesive material, metal particles and a conductive filler are added is suitable.

[0164]

Referring to the drawings again, in Fig. 17, Dx1 to Dxm and Dy1 to Dyn and Hv designate terminals for electrical connection of a hermetic structure provided to electrically connect the display panel to electric circuits not shown in the figure. Dx1 to Dxm, Dy1 to Dyn and Hv electrically connect with the row wiring 1013 of the multiple electron beam source, the column wiring 1014 of the multiple electron beam source and the metal back 1019 of the face plate, respectively.

[0165]

In order to evacuate the hermetic container, an exhaust tube and a vacuum pump, both of which are not shown in the figure, are connected to each other after the hermetic container is assembled. The hermetic container is evacuated to the vacuum degree of about 10^{-7} [Torr]. The exhaust tube is to be sealed after the evacuation, immediately before or after the sealing, however, a getter film (not shown in the figure) is formed in a prescribed position within the hermetic container to maintain the vacuum degree within the container. A getter film means a film formed by subjecting a getter material whose main component is Ba to heating with a heater or high-frequency heating and evaporation. Due to the adsorption of the above getter film, the vacuum degree inside the hermetic container is kept 1×10^{-5} to 1×10^{-7} [Torr].

[0166]

In the image displays using the display panel described above, electrons are emitted from each of the cold cathode devices 1012 when applying a voltage to each of the devices 1012 through the terminals Dx1 to Dxm and Dy1 to Dyn outside the container. When applying a voltage of from several hundreds volt [V] to several kilovolt [kV] to the metal back 1019 through the terminal Hv outside the container while applying a voltage to each device 1012, the above emitted electrons are accelerated and collide against the inner surface of the face plate 1017. This excites the differently colored fluorescent substances constituting the fluorescent film 1018 and allows them to emit light, which leads to displaying images.

[0167]

Normally, the voltage applied to the surface conduction electron emission device 1012, which is a cold cathode device, of the present invention is from about 12 to 16 [V], the distance d of the metal back 1019 from the cold cathode electrode 1012 is from about 0.1 [mm] to 8 [mm], and the voltage between the metal back 1019 and the cold cathode electrode 1012 is from about 0.1 [kV] to 10 [kV].

[0168]

The basic construction of the display panel embodying the present invention and the production

method thereof as well as the rough summary of the image display have been described above.

[0169]

Now the method of producing a multiple electron beam source used for the display panel of the above embodiment will be described. Any multiple electron beam sources can be used for the image display of the present invention as long as multiple cold cathode devices are arranged in a simple matrix and wired or they are arranged in a ladder form and wired. The material, shape and production method of the cold cathode devices are not restricted at all. Thus, cold cathode devices such as surface conduction electron emission devices, FE type devices or MIM type devices are all applicable.

[0170]

Among these types cold cathode devices, however, the surface conduction electron emission devices are especially preferable, if an image display is required such that its display screen is large and its price is low. Specifically, in FE type devices, their electron emission properties are largely dependent on the relative position of an emitter cone and a gate electrode as well as their shape, consequently their production technique requires an extremely high accuracy. This is a disadvantageous factor when trying to achieve an enlarged display screen or a reduced

production cost. In MIM type devices, it is required that the film thickness of the insulating layer and the upper electrode should be thin and uniform. This is also a disadvantageous factor when trying to achieve an enlarged display screen or a reduced production cost. In that respect, in the surface conduction electron emission devices, their production method is relatively simple, therefore, it is easy to obtain an enlarged display screen and reduce the production cost. Further, it has been found by the present inventors that, among the surface conduction electron emission devices, the one whose electron emission portion or its periphery is formed with fine-particle film is especially excellent in electron emission properties and easy to produce. Accordingly, the above one can be said to be most suitable for use in the multiple electron beam sources of image displays having a high luminance and a large screen. Thus, in the display panel of the above embodiment were used the surface conduction electron emission devices whose electron emission portion or its periphery is formed with fine-particle film. Now the basic construction of the suitable surface conduction electron emission devices, the production method thereof and the characteristics thereof will be described, followed by describing the structure of the multiple electron beam source in which multiple devices are wired in a simple matrix.

[0171]

[Suitable Construction of Surface conduction electron emission devices and Method of Producing Thereof]

There are two types of typical construction of surface conduction electron emission devices in which the electron emission portion or its periphery is formed of fine-particle film: planar type and vertical type.

[0172]

[Planar Surface conduction electron emission devices]

First, the construction of planar surface conduction electron emission devices and the production method thereof will be described. Fig. 19 shows a plan view (a) illustrating a construction of a planar surface conduction electron emission device and a sectional view (b) illustrating the same. In the Figures, reference numeral 1011 designates a substrate, numerals 1102 and 1103 device electrodes, 1104 a conductive thin film, 1105 an electron emission portion formed by the energization forming processing, and 1113 a film formed by the energization activation processing.

[0173]

For the substrate 1011, various types glass substrates including, for example, quartz glass and green sheet glass, various types ceramics substrates

including alumina, or the above various types substrates with an insulating layer of, for example, SiO_2 laminated thereon can be used.

[0174]

The device electrodes 1102 and 1103 provided opposite to each other on the substrate 1011 parallel thereto are formed of conductive materials. The material may be properly selected from the group consisting of metals including, for example, Ni, Cr, Au, Mo, W, Pt, Ti, Cu, Pd and Ag or their alloys, metal oxides including In_2O_3-SnO_2, semi-conductor such as poly-silicon and so on. The device electrodes 1102 and 1103 can be easily formed by combining the film formation technique such as vacuum deposition and the patterning technique such as photolithography and etching, however the other techniques (for example, printing technique) may also be used.

[0175]

The shape of the device electrodes 1102 and 1103 is properly designed to suit for the purpose of applying the electron emission device concerned. Generally, the devices are usually designed in such a manner that the electrodes are spaced at intervals ranging from several hundreds Å to several hundreds µm. In order to apply the devices to an image display, preferably the intervals are selected in the range of several µm to several tens µm. The thickness of the

device electrodes d is properly selected among the values ranging from several hundreds Å to several μm.

[0176]

In the portion of the conductive thin film 1104, fine-particle film is used. The fine-particle film mentioned herein means the film containing multiple fine particles (including island-shaped aggregation) as a component. When microscopically examining the fine-particle film, the structure is observed where individual fine particles are spaced at certain intervals, or they are adjacent to each other, or they are overlapping with each other.

[0177]

The diameter of the fine particles used in the fine-particle film is in the range of several Å to several thousands Å, preferably in the range of 10 Å to 200 Å. The thickness of the fine-particle film is properly set considering the conditions described below. That is, the conditions required under which the film is electrically satisfactorily connected with the device electrodes 1102 and 1103, the conditions required under which the film satisfactorily undergoes energization forming, the conditions required under which the electric resistance of the film itself has a proper value as described below, and so on. In particular, the thickness of the fine-particle film is set for any one of the values ranging from several A to

several thousands A, preferably any one of the values ranging from 10 Å to 500 Å.

[0178]

The materials may be used in the formation of the fine-particle film is properly selected from the group consisting of, for example, metals including Pd, Pt, Ru, Ag, Au, Ti, In, Cu, Cr, Fe, Zn, Sn, Ta, W and Pb, oxides including PdO, SnO_2, In_2O_3, PbO and Sb_2O_3, borides including HfB_2, ZrB_2, LaB_6, CeB_6, YB_4 and GdB_4, carbides including TiC, ZrC, HfC, TaC, SiC and WC, nitrides including TiN, ZrN and HfN, semi-conductor including Si and Ge, and carbone.

[0179]

The conductive thin film 1104 is formed of fine-particle thin film, as described above, and its sheet resistivity is set for any one of the values ranging from 10^3 to 10^7 $\Omega/\square$.

[0180]

Since it is desirable that the conductive thin film 1104 and the device electrodes 1102 and 1103 are electrically satisfactorily connected, the structure of the devices is designed in such a manner that both of them partly overlap with each other. The substrate, the device electrodes and the conductive thin film are laminated in this ascending order in the example shown in Fig. 19, however, the substrate, the conductive thin film and the device electrodes may be laminated in this

ascending order depending on the situation.

[0181]

The electron emission portion 1105 is the crack-shaped portion formed on a part of the conductive thin film 1104 and electrically more resistive than its surroundings. The crack is formed by subjecting the conductive thin film 1104 to energization forming processing describe below. There are cases in which the fine particles of several Å to several hundreds Å in diameter are arranged in the crack. Incidentally, it is very difficult to illustrate the details of the position and shape of the actual electron emission portion precisely and exactly, therefore, they are schematically shown in Fig. 19.

[0182]

The thin film 1113 is a film formed of carbon or its compound which coats the electron emission portion 1105 and its vicinities. The thin film 1113 is formed by subjecting the conductive thin film 1104 to energization activation processing after energization forming processing.

[0183]

The thin film 1113 is formed of any one of single crystal graphite, polycrystal graphite and noncrystalline carbon, or the mixture thereof, and its thickness is preferably 500 [Å] or lower, more preferably 300 [Å] or lower. Incidentally, it is very

difficult to illustrate the details of the position and shape of the actual thin film 1113, therefore, they are schematically shown in Fig. 19. In the plan view (a), the device is shown with the part of the thin film 1113 (the upper layer above 1105) removed.

[0184]

The basic construction of preferred devices has been described above, and in the preferred embodiments used were the devices described below.

[0185]

That is, for the substrate 1011 used was green sheet glass and for the device electrodes 1102 and 1103 used was Ni thin film. The thickness d of the device electrodes 1102 and 1103 was 1000 [Å], and their interval L was 2 [µm].

[0186]

For the main material of the fine-particle film used was Pd or PdO, and the thickness and width W of the fine-particle film were 100 [Å] and 100 [µm], respectively.

[0187]

Now the method of producing preferable planar surface conduction electron emission devices will be described. Referring to the drawings, (a) to (e) of Fig. 24 are sectional views illustrating the process of producing of surface conduction electron emission devices. The reference numeral of each member

corresponds to that of Fig. 19 described above.

[0188]

1) First, the device electrodes 1102 and 1103 are formed on the substrate 1011 as shown in (a) of Fig. 24.

[0189]

The substrate 1011 is cleaned sufficiently using a cleaning agent, deionized water and an organic solvent prior to forming the electrodes, then the material of device electrodes is deposited thereon. As a method of deposition, vacuum film formation techniques such as vacuum deposition, sputtering and so on are applicable. Succeedingly, the electrode material deposited is patterned using photolithography/etching techniques so as to form a pair of device electrodes 1102 and 1103 shown in (a) of Fig. 24.

[0190]

2) Second, the conductive thin film 1104 is formed, as shown in (b) of Fig. 24.

[0191]

When forming the thin film 1104, first the substrate shown in (a) of Fig. 24 is subjected to application of organic metal solution and drying, then a fine-particle thin film is formed thereon by heat firing processing, after which the thin film is patterned into a prescribed form by photolithography/etching. The organic metal solution mentioned herein means a solution of an organic metal

compound of that main device is the same as the fine-particle material used in the conductive thin film. In particular, the main device used in the present embodiment was Pd. Although dipping process was used in the present embodiment as an application process, the other processes, for example, spinner process and spray process, are also applicable.

[0192]

As a method of forming the conductive thin film 1104 of fine-particle film, the methods other than the one used in the present embodiment in which an organic metal solution is applied to the substrate, for example, vacuum deposition, sputtering and chemical vapor phase deposition can be used.

[0193]

3) The electron emission portion 1105 is formed by conducting energization forming in which a proper voltage is applied between the device electrodes 1102 and 1103 through the forming source 1110 as shown in (c) of Fig. 24.

[0194]

Energization forming processing means that the conductive thin film 1104 formed of fine-particle film is energized to undergo a proper fracture, deformation or change in quality in a part thereof, so that its structure is suitably changed. In the portion of the conductive thin film formed of fine-particle film whose

structure has undergone a change suitable for performing electron emission (that is, the electron emission portion 1105), the thin film has a proper crack formed on it. The electric resistance measured between the device electrodes 1102 and 1103 substantially increases after the electron emission portion 1105 is formed as compared with before its formation.

[0195]

In order to explain the energization processing more in detail, one example of the waveforms of a proper voltage applied through the forming source 1110 is shown in Fig. 25. When subjecting the conductive thin film 1104 formed of fine-particle film to the forming processing, preferably a pulse voltage is applied to the film. And in the present embodiment a triangular pulse voltage with a pulse width of T1 and a pulse spacing of T2 is continuously applied to the conductive thin film as shown in Fig. 16. In that case, the peak value of the triangular pulse voltage Vpf is increased step by step. A monitor pulse Pm for monitoring the state in which the electron emission portion 1105 is formed is inserted between the triangular pulses at a proper interval, and the current flow was measured with an ammeter 1111.

[0196]

In the present embodiment, the peak value Vpf was

adjusted in 0.1 [V] increments for each pulse under a vacuum atmosphere of the order of, for example, 10^{-5} [Torr] while setting, for example, the pulse width T1 for 1 [msec] and pulse spacing T2 for 10 [msec]. The monitor pulse Pm was inserted once per every five triangular pulses. The voltage of the monitor pulse Vpm was set for 0.1 [V] in order not to affect the forming processing. The energization involved in the forming processing was terminated at the stage where the electric resistance between the device electrodes 1102 and 1103 became 1×10^{6} [Ω], that is, the current measured with the ammeter 1111 while applying the monitor pulse became 1×10^{-7} [A].

[0197]

The above method is preferable with respect to the surface conduction electron emission devices of the present embodiment; accordingly, if the design of the surface conduction electron emission devices, such as the material or thickness of the fine-particle film or the intervals L of the device electrodes, is changed, desirably the energization conditions are properly changed.

[0198]

4) The electron emission properties are improved by conducting an energization activation processing in which a proper voltage is applied between the device electrodes 1102 and 1103 using an activation source

1112 as shown in (d) of Fig. 24.

[0199]

The energization activation processing means that carbon or its compound is caused to deposit in the vicinity of the electron emission portion 1105, which is formed by the above energization forming processing, by subjecting the portion to energization under proper conditions. (In the Figure, the deposition of carbone or its compound is schematically shown as a member 1113.) Typically, the energization activation processing provides a 100-fold or more increase in emission current as compared with before conducting the processing.

[0200]

In particular, carbon or its compound originated from the organic compounds existing in a vacuum atmosphere is deposited in the vicinity of the electron emission portion 1105 by applying voltage pulses to the portion at regular intervals under a vacuum atmosphere within the range of 10^{-5} to 10^{-4} [Torr]. The deposition 1113 is any one of single crystal graphite, polycrystal graphite and non-crystalline graphite, or the mixture thereof, and its thickness is preferably 500 [Å] or smaller, more preferably 300 [Å] or smaller.

[0201]

In order to explain the energization processing more in detail, one example of the waveforms of a

proper voltage applied through the activation source 1112 is shown in (a) of Fig. 26. In the present embodiment, the energization activation processing was conducted by applying a rectangular wave of a certain voltage at regular intervals. In particular, the voltage of the rectangular wave Vac was 14 [V], the pulse width T3 was 1 [msec] and the pulse spacing T4 was 10 [msec]. The above energization conditions are preferable with respect to the surface conduction electron emission devices of the present embodiment; accordingly, if the design of the surface conduction electron emission devices is changed, desirably the conditions are properly changed.

[0202]

Referring to the drawings, reference numeral 1114 shown in (d) of Fig. 24 designates an anode electrode for capturing the emission current Ie emitted from the above surface conduction electron emission device, and it is connected with a direct current high voltage source 1115 and an ammeter 1116. (In cases where the activation processing is conducted after incorporating the substrate 1011 into the display panel, the fluorescent surface of the display panel is used as an anode electrode 1114.) While applying a voltage from the activation source 1112, the progress of the energization activation processing is monitored by measuring the emission current Ie with the ammeter 1116

and the operation of the activation source 1112 is controlled. One example of the emission currents Ie measured with the ammeter 1116 is shown in (b) of Fig. 26. When starting to apply a pulse voltage from the activation source 1112, the emission current Ie increases with time, but it becomes saturated before long and comes to hardly increase. The energization activation processing is terminated at a time when the emission current Ie is almost saturated by stopping the application of the voltage from the activation source.

[0203]

Incidentally, the above energization conditions are preferable with respect to the surface conduction electron emission devices of the present embodiment; accordingly, if the design of the surface conduction electron emission devices is changed, desirably the conditions are properly changed.

[0204]

The planar surface conduction electron emission device shown in (e) of Fig. 24 was thus produced.

[0205]

[Vertical Surface conduction electron emission devices]

Now, another typical construction of surface conduction electron emission devices whose electron emission portion or periphery is formed with fine-particle film, that is, the construction of vertical

surface conduction electron emission devices will be described.

[0206]

Referring to the drawings, Fig. 27 is a sectional view of a vertical surface conduction electron emission device illustrating its basic construction. In the figure, reference numeral 1201 designates a substrate, each of numerals 1202 and 1203 an device electrode, numeral 1206 a step formation member, numeral 1204 a conductive thin film using fine particles film, numeral 1205 an electron emission portion formed by conducting energization forming processing, and numeral 1213 a thin film formed by conducting energization activation processing.

[0207]

The vertical type differs from the planar type in that one of the device electrodes (1202) is provided on the step formation member 1206 and one of the side surfaces of the step formation member 1206 is coated with the conductive thin film 1204. Accordingly, the intervals of the device electrodes L in the planar type shown in Fig. 19 is set as a step height L of the step formation member 1206 in the vertical type. As for the materials of the substrate 1201, device electrodes 1202 and 1203, and the conductive thin film 1204 using fine-particle film, the materials listed in the description of the above planar type are applicable. For the step

formation member 1206, an electrically insulating material such as SiO_2 is used.

[0208]

Now, the method of producing vertical surface conduction electron emission devices will be described. Referring to the drawings, (a) to (f) of Fig. 28 are sectional views for illustrating the production process of the vertical surface conduction electron emission devices, and reference numerals of each member designate the same member as in Fig. 27 described above.

[0209]

1) A device electrode 1203 is formed on the substrate 1201 as shown in (a) of Fig. 28.

[0210]

2) An insulating layer for forming the step formation member on it is laminated as shown in (b) of Fig. 28. While the insulating layer is laminated with, for example, SiO_2 by sputtering, the other film formation processes such as vacuum deposition and printing process are also applicable.

[0211]

3) A device electrode 1202 is formed on the insulating layer as shown in (c) of Fig. 28.

[0212]

4) Part of the insulating layer is removed by, for example, an etching method so as to expose the device electrode 1203, as shown in (d) of Fig. 28.

[0213]

5) A conductive thin film 1204 using fine-particle film is formed as shown in (e) of Fig. 28. For this film formation, film formation techniques such as application process can be used, like the above planar type.

[0214]

6) Like the above planar type, an electron emission portion is formed by conducting energization forming processing. (The similar energization forming processing as described using (c) of Fig. 24 may be conducted.)

7) Like the above planar type, carbon or its compound is caused to deposit in the vicinity of the electron emission portion by conducting energization activation processing. (The similar energization activation processing as described using (d) of Fig. 24 may be conducted.)

The vertical surface conduction electron emission device shown in (f) of Fig. 28 was thus produced.

[0215]

[Properties of Surface conduction electron emission devices used in Image Producer]

The construction of the planar and vertical surface conduction electron emission devices and the production method thereof have been described, and now the properties of the devices used in an image display

will be described.

[0216]

Referring to the drawings, Fig. 29 shows typical examples of (Emission Current Ie) to (Device Voltage Vf) and (Device Current If) to (Device Voltage Vf) properties. The emission current Ie is significantly small as compared with the device current If, therefore, it is very difficult to illustrate them with the identical scale, in addition, the above properties change with changes in design parameter, such as size of device, shape of the same and so on. Thus, the two properties are illustrated in their respective desired units.

[0217]

The devices used in an image display have three properties described below, related to emission current Ie.

[0218]

First, the emission current Ie rapidly increases when the voltage equal to or higher than the voltage of a certain value (referred to as "threshold voltage Vth") is applied to the devices, while it is hardly detected when the voltage lower than the threshold voltage Vth is applied.

[0219]

That is, the devices are non-linear devices having a definite threshold Vth with respect to the emission

current Ie.

[0220]

Second, the emission current Ie varies depending on the voltage Vf applied to the devices, therefore, the magnitude of the emission current Ie can be controlled by the voltage Vf.

[0221]

Third, the current Ie emitted from the devices quickly responds to the voltage Vf applied thereto, therefore, the amount of charge of the electrons emitted from the devices can be controlled by the duration time of applying the voltage Vf.

[0222]

The surface conduction electron emission devices were suitably applied to an image display due to the above properties. For example, in the image display in which multiple devices are provided corresponding to the picture devices of its display screen, display is made possible by scanning the display screen in turn while taking advantage of the first property. That is, the voltage equal to or higher than the threshold voltage Vth is applied to the devices under drive according to the desired luminance, while the voltage lower than the threshold voltage Vth is applied to the devices in the non-selective state. Display is made possible by scanning the display screen in turn while switching the devices to be driven in turn.

[0223]

Further, the luminance of the display screen can be controlled while taking advantage of the second or the third property, which makes possible a gradation display.

[0224]

[Structure of Multiple Electron Beam Source with Multiple Devices Arranged in a Simple Matrix]

Now, the structure of a multiple electron beam source will be described in which the above surface conduction electron emission devices are wired in a simple matrix.

[0225]

Referring to the drawings, Fig. 20 is a plan view of the multiple electron beam used in the display panel of Fig. 17 described above. On the substrate 1011, arranged are the same surface conduction electron emission devices 1012 as shown in Fig. 19, which are wired in a simple matrix with row wiring electrodes 1003 and column wiring electrodes 1004. On each portion where a row wiring electrode 1003 and a column wiring electrode 1004 intersect, an insulating layer (not shown in the figure) is formed between the electrodes to keep them electrically insulating.

[0226]

Fig. 21 is a sectional view of the multiple electron beam source of Fig. 20, taken along the line

B-B'.

[0227]

The multiple electron beam source having such a structure was produced by first forming the row wiring electrodes 1013, the column wiring electrodes 1014, the insulating layers between the electrodes (not shown in the figure), the device electrodes of the surface conduction electron emission devices 1012 and the conductive thin film on the substrate, then conducting energization forming processing and energization activation processing while feeding power to each device via the row wiring electrodes 1013 and the column wiring electrodes 1014.

[0228]

[Construction of Driving Circuit (and Driving Method thereof)]

Referring to drawings, Fig. 30 is a block diagram schematically showing a configuration of driving circuit for displaying a television screen based on the NTSC television signals. In the figure, a display panel designated by reference numeral 1701 corresponds to the display panel described above, and it is produced and operates in the same manner as described above. A scanning circuit designated by numeral 1702 scans scanning lines, and a control circuit 1703 generates signals and the like input into the scanning circuit 1702. A shift register 1704 shifts data of

each line, and a line memory 1705 outputs the data for one line from the shift register 1704 to a modulation signal generator 1707. A synchronizing signal separating circuit 1706 separates the synchronizing signals from NTSC signals.

[0229]

The functions of each part of the circuit shown in Fig. 30 will be described in detail below.

[0230]

The display panel 1701 is connected with an external electric circuit via terminals Dx1 to Dxm, terminals Dy1 to Dyn and a high voltage terminal Hv. To the terminals Dx1 to Dxm, applied are scanning signals for driving the multiple electron beam source provided in the display panel 1701, that is, for driving the cold cathode devices wired in a matrix of m rows and n columns one by one (n devices). On the other hand, to the terminals Dy1 to Dyn, applied are modulation signals for controlling the output electron beam of each of n devices for one row selected by the above scanning signals. And to the high voltage terminal Hv, a DC voltage of, for example, 5 [kV] is supplied from a DC voltage source Va. The above voltage means an accelerating voltage for providing a sufficient energy for the excitation of fluorescent substances to the electron beam output from the multiple electron beam source.

[0231]

Then the scanning circuit 1702 will be described. The scanning circuit 1702 has m switching devices (in the figure, they are schematically shown by S1 to Sm) in it, and each of the switching devices selects either one of the output voltage of an DC voltage Vx and 0 [V] (GND level) and electrically connects with the terminals Dx1 to Dxm of the display panel 1701. Each switching device, S1 to Sm, operates according to the control signals Tscan output from the control circuit 1703, and actually it can be easily constructed by combining the switching devices like FET. The above DC voltage source Vx is set so that it will output a certain voltage to keep the driving voltage applied to the devices having been not scanned at a level equal to or lower than the electron emission threshold voltage Vth based on the properties of the electron emission devices illustrated in Fig. 29.

[0232]

The control circuit 1703 has a function of coordinating the operations of each part so that an appropriate display will be made based on the image signals input from the outside. It generates control signals Tscan, Tsft and Tmry toward each part based on the synchronizing signals Tsync sent from a synchronizing signal separation circuit 1706 described below. The synchronizing signal separation circuit

1706 is a circuit for separating a synchronizing signal component and a luminance signal component from a NTSC television signal input from the outside. Although the synchronizing signal separated by a synchronizing signal separation circuit 1706 consists of a vertical synchronizing signal and a horizontal synchronizing signal, as is well known, it is shown as a Tsync signal in the figure for convenience. On the other hand, the luminance signal component of an image separated from the above television signal is referred to as DATA signal for convenience, and the signal is input into a shift register 1704.

[0233]

The shift register 1704 is a register for subjecting the above DATA signal input into serial on the basis of time series to serial/parallel conversion for each image line, and it operates based on the control signal Tsft sent from the control circuit 1703. In other words, the control signal Tsft can be a shift lock of the shift register 1704. The data for 1 line of image subjected to serial/parallel conversion (corresponds to the driving data of n electron emission devices) are output from the above shift register 1704 as n signals of Id1 to Idn.

[0234]

A line memory 1705 is a memory for storing the data for 1 line of image for a required period time,

and it stores properly the contents of Id1 to Idn in accordance with control signal Tmry sent from the control circuit 1703. The contents stored are output as I'd1 to I'dn and input into a modulation signal generator 1707.

[0235]

The modulation signal generator 1707 is a signal source for driving and modulating each of the electron emission devices 1012 according to each of the image data I'd1 to I'dn, and its output signal is applied to the electron emission devices 1015 within the display panel 1701 through the terminals Dy1 toDyn.

[0236]

As described above using Fig. 29, the surface conduction electron emission devices in accordance with the present invention has basic properties described below for emission current Ie. That is, there exists a definite threshold voltage Vth in electron emission (in the case of the surface conduction electron emission device described in the embodiment below, Vth is 8 [V]), electrons are emitted only when applying a voltage equal to or higher than the threshold voltage Vth. And under the voltage higher than the threshold voltage Vth, emission current Ie changes with changes in voltage as shown in the graph of Fig. 29. This means that, in cases where a panel voltage is applied to the devices of the present invention, when applying a voltage lower

than the threshold voltage Vth, electron emission does not occur, on the other hand, when applying a voltage higher than the threshold voltage Vth, electron beam is output from the surface conduction electron emission devices. Changing the peak value of the pulse Vm at that time makes possible controlling the intensity of the output electron beam. Further, changing the pulse width Pw makes possible controlling the total amount of charges of the output electron beam.

[0237]

Thus, as a method of modulating electron emission devices according to input signals, a voltage modulation method, a pulse width modulation method and the like can be adopted. When executing the voltage modulation method, a circuit of a voltage modulation method in which a certain length of voltage pulse is generated and the peak value of the pulse is properly modulated in accordance with the data input can be used as a modulation signal generator 1707. When executing the pulse width modulation method, a circuit of a pulse width modulation type in which a certain peak value of voltage pulse is generated and the pulse width of the voltage is properly modulated in accordance with the data input can be used as a modulation signal generator 1707.

[0238]

For the shift register 1704 and the line memory

1705, either a digital signal type or an analog signal type can be adopted. That is, it does not matter which type should be adopted as long as the serial/parallel conversion of an image signal and storing are conducted at a prescribed rate.

[0239]

When using a digital signal type, though it is necessary that the output signal DATA from the synchronizing signal separation circuit 1706 is converted into digital signals, this can be done if only an A/D converter is provided at the output portion of the synchronizing signal separation circuit 1706. In connection with this, the circuit used for the modulation signal generator varies depending on whether the output signals of the maim memory 115 is digital or analog. Specifically, in case of the voltage modulation method using digital signals, for example, an D/A conversion circuit is used for the modulation signal generator 1707, and an amplification circuit or the like is added if necessary. In case of the pulse width modulation method, a circuit combined with a counter for counting the number of waves output from a high-speed oscillator or an oscillator and a comparator for comparing the output values of the counter and the above memory is used for modulation signal generator 1707. If necessary, an amplifier can be added for amplifying the voltage of the signals subjected to a

pulse width modulation and output from the comparator to the driving voltage of the electron emission devices.

[0240]

In case of the voltage modulation method using analog signals, for example, an amplification circuit using an operational amplifier is adopted for the modulation signal generator 1707, and a shift-level circuit or the like may be added if necessary. In case of the pulse width modulation method, a voltage controlling type oscillation circuit (VCO) can be adopted. If necessary, an amplifier can be added for amplifying the voltage to the driving voltage of the electron emission devices.

[0241]

In a image display to which the present invention having such a construction is applicable, electrons are emitted by applying a voltage to each of the electron emission devices via terminals, Dx1 to Dxm and Dy1 to Dyn, outside the container. The electron beam is accelerated as a result of applying a high voltage to the metal back 1019 or the transparent electrode (not shown in the figures) via the high voltage terminal Hv. The accelerated electrons collide with the fluorescent film 1018, which causes light emission and consequently produces an image.

[0242]

[Electron Beam Source having a Ladder-shaped

Arrangement]

Now an electron source substrate having a ladder-shaped arrangement and an image display using the same will be described with reference to Figs. 31 and 32.

[0243]

Referring to Fig. 31, reference numeral 1011 designates an electron source substrate, numeral 1012 electron emission devices, and Dx1 to Dx10 of numeral 1126 common wiring connecting with the above electron emission devices. Multiple electron emission devices 1012 are arranged in parallel with a row in the direction of X on the substrate 1011. (this is referred to as device row). An electron source substrate having a ladder-shaped arrangement is produce by arranging multiple device rows on the substrate. Each of the device rows can be driven independently by properly applying a driving voltage between the common wiring of each device row. Specifically, a voltage higher than the threshold voltage Vth is applied to the device rows from which electron beam is to be emitted, and a voltage lower than the threshold voltage Vth is applied to the device rows from which no electron beam is to be emitted. The common wiring, for example, Dx2 and Dx3 of Dx2 to Dx9 may be the same wiring.

[0244]

Fig. 32 shows a structure of an image display provided with an electron source having a ladder-shaped

arrangement. Reference numeral 1120 designates grid electrodes, 1121 pores for allowing electrons to pass through, 1122 terminals outside of the container consisting of Dox1, Dox2, ... Dox, 1123 terminals outside of the container consisting of G1, G2, ... Gn connecting with the grid electrodes 1120, 1011 an electron source substrate in which each common wiring between the device rows is the same. The same reference numerals in Figs. 31 and 32 designate the same member. The difference between this type image producer and the image producer in a simple matrix arrangement (Fig. 17) is that this type image producer has grid electrodes 1120 provided between the electron source substrate 1011 and the face plate 1017.

[0245]

In the panel structure described above, spacers 120 can be provided between the face plate 1017 and the rear plate 1015, if necessary in terms of its atmospheric-pressure structure, in both cases where the devices are arranged in a simple matrix and in a ladder-shaped form.

[0246]

In the middle position between the substrate 1011 and the face plate 1017, provided are grid electrodes 1120. The grid electrodes 1120 can modulate the electron beam emitted from the surface conduction electron emission devices 1012, and each grid electrode

is provided with circular openings 1121 corresponding to each device to allow electron beam to pass through the electrodes provided in stripes perpendicular to the device rows in a ladder-shaped arrangement. The shape of the grids and the installation position thereof are not limited to those of Fig. 32. Multiple through-holes, as an opening, can be provided in a mesh form, and they can be provided around or in the vicinity of the surface conduction electron emission devices.

[0247]

The terminals 1122 outside the container and the grid terminals 1123 outside the container are electrically connected with the driving circuit shown in Fig. 30.

[0248]

In the present image display, the exposure of the fluorescent substances to each electron beam can be controlled by applying modulation signals for 1 line of image to the grid electrodes and driving (scanning) the device rows line by line synchronously. Thus the image can be displayed line by line.

[0249]

The construction of the above two image displays is an example of the image producers to which the present invention is applicable, and various changes and modifications can be made in it based on the concept of the present invention. Input signals have

been described in terms of NTSC, they are, however, not limited to this, PAL method, SECAM, and TV signals (for example, high definition television) consisting of a larger number of scanning lines as compared with the former can also be adopted.

[0250]

In accordance with the present invention, image producers for television broadcasting as well as image producers suitable for the image displays of video conference system, computers and the like can be provided. In addition, image producers as an optical printer comprising of a photographic drum can be provided.

[0251]

[Examples]

The present invention will be explained more detail with reference to the concrete examples.

[0252]

In the respective examples described below, used was the multiple electron beam source of a type in which N × M (N = 3072, M = 1024) surface conduction electron emission devices having an electron emission portion on the conductive fine-particle film between electrodes are wired in a matrix with M direction rows of wiring and N direction columns of wiring (refer to Figs. 17 and 20).

[0253]

[Example 1] Glass Substrate/Aluminum Sputtering Film/Anodic Oxidation Micro-hole

The spacer 1024 used in this example was produced as described below.

[0254]

As a master, a soda-lime glass substrate which was the same material as the rear plate was used. The master was subjected to shape processing by injection molding and mirror finish polishing so that its outside dimensions of the thickness, height and length would be 0.2 mm, 3 mm and 40 mm, respectively. The average roughness of the substrate surface thus formed was 100 Å. Hereinafter, the substrate will be referred to as g0.

[0255]

Prior to deposition process, the above spacer substrate g0 was subjected to first ultrasonic cleaning in deionized water, isopropyl alcohol (IPA) and acetone for 3 minutes, then drying at 80°C for 30 minutes, and followed by UV ozone cleaning so as to remove organic residues on the surface of the substrate.

[0256]

Then titanium and aluminium were deposited on each side of the substrate by sputtering so as to form films 0.5 μm and 0.1 μm, respectively. After that, the substrate was subjected to anodic oxidation treatment in 0.3 N oxalic acid aqueous solution. The

electrolytic conditions in that case were such that the voltage applied to anode was 40 V and energization time was 30 minutes in a potensional mode. By this electrolytic treatment, micro-holes of average diameter 1000 Å and the maximum depth 5000 Å were formed with the adjacent holes spaced at average intervals of 2000 Å.

[0257]

In order to provide unevenness on the top surface portion, the surface of the substrate was subjected to processing with #4000 sandpaper and made rough. The average roughness of the non-opening portion was 100 A then. Hereinafter the substrate thus obtained is referred to as substrate g1. The appearance of the surface of the substrate g1 is roughly as follows: the surface aluminium layer was turned into an insulating alumina layer in a highly oxidized state, there existed micro-holes which were almost uniformly spaced as a whole and reached the titanium layer at the bottom, and infinitesimal unevenness was formed in every pore.

[0258]

Then a Cr-Al alloy nitride film of 200 nm, as an antistatic film, was formed on the surface of the substrate by subjecting Cr and Al targets to sputtering with a high-frequency power source. The sputtering gas used was a mixed gas with Ar-to-N_2 ratio of 1 : 2 and its total pressure was 1 mTorr (0.13 Pa). For the film

co-deposited under the above conditions, the sheet resistivity was □ = 2×10^9 Ω/□.

[0259]

The antistatic film applicable to the present invention is not limited to this, various types antistatic film are applicable.

[0260]

Further a low resistive film was formed in the region to become an upper-lower electrodes junction portion by the method described below. The above region was subjected to vapor phase deposition to form a titanium film of 10 nm thickness and a Pt film of 200 nm thickness in a 200 μm sheet form parallel to the above junction portion by sputtering. The Ti film was needed as a foundation layer for reinforcing the film adhesion of the Pt film. The spacer 1020 with a low resistive film was thus obtained. Hereinafter thus obtained spacer is referred to as spacer A. The film thickness of the low resistive film was 210 nm, and the sheet resistivity was 10 Ω/□.

[0261]

Fig. 3 shows the surface geometry of the highly resistive film of spacer A thus obtained.

[0262]

In the above uneven portion, the coating performance of the film was satisfactory over the boundary regions between the depressed portion and the

elevated portion, and the opening regions of the substrate were not filled up by the formation of the highly resistive film. Further, in the non-opening regions, the continuity of the film was satisfactory.

[0263]

The incident angle dependency coefficient of secondary electron emission coefficient m_0 of spacer A was 2 for the incident electron energy of 1 keV.

[0264]

In the present example, a display panel was produced in which the spacers 1020 shown in Fig. 17 were arranged. The details will be described with reference to Figs. 17 and 18. First, the substrate 1011 with row wiring electrodes 1013, column wiring electrodes 1014, insulating layers between electrodes (not shown in the figures) and the device electrode and conductive thin film of the surface conduction electron emission devices 1012 formed on it was fixed on the rear plate 1015. Then the above spacers A, as a spacer 1020, were fixed on the row wiring electrodes 1013 of the substrate 1011 at regular intervals and parallel thereto. After that, a face plate 1017 with a fluorescent film 1018 and a metal back 1019 provided on its internal surface was arranged 5 mm above the substrate 1011 via side walls 1016, and the rear plate 1015, the face plate 1017, the side walls 1016 and the spacers 1020 were fixed at each junction portion. Frit

glass (not shown in the figures) was applied to the substrate 1011 - rear plate 1015 junction, the rear plate 1015 - side wall 1016 junction and the face plate 1017 - side wall 1016 junction, and each of the junction portions was sealed by firing at 400°C to 500°C in the atmosphere for 10 minutes or longer. The spacers 1020 were arranged with their one side facing the substrate 1011 being on the row wiring 1013 (of 300 μm width) and the other side facing the face plate 1017 being on the metal back 1019 via a conductive filler or a conductive frit glass (not shown in the figures) mixed with a conductive material such as metals (not shown in the figures). And their adhesion and electrical connection were achieved by firing them at 400°C to 500°C in the atmosphere for 10 minutes or longer at the same time that the above hermetic container was sealed.

[0265]

In the present example, adopted was the fluorescent film 1018 which was formed, as shown in Fig. 23, in such a manner that fluorescent substances 1301 of the same color were placed in a column (in the direction of Y), multiple columnar lines of different colors form stripes, and black conductors 1010 are arranged between the two differently colored fluorescent substances (R, G, B) 1301 as well as between the two consecutive picture devices of the same

color placed in the direction of Y. And the spacers 1020 were arranged within the region (of 300 μm width) parallel to each row of the black conductors 1010 (in the direction of X) via the metal back 1019. When conducting the sealing described above, the rear plate 1015, the face plate 1017 and the spacer 1020 were carefully positioned so that the each differently colored fluorescent substance 1301 will correspond to each device 1013 arranged on the substrate 1011.

[0266]

After the hermetic container thus completed was evacuated with a vacuum pump through an exhaust tube (not shown in the figures) till it had a sufficient vacuum degree, the aforementioned energization forming processing and energization activation processing were conducted by feeding power to each device 1013 via the row wiring electrodes 1013 and the column wiring electrodes 1014 through the terminals Dx1 to Dxm and Dy1 to Dyn outside the hermetic container. A multiple electron beam source was thus produced. Then the outer enclosure (hermetic container) was sealed by heating the exhaust tube not shown in the figures with a gas burner to be deposited with vacuum degree of 10^{-6} [Torr].

[0267]

Finally, a getter processing was conducted to maintain the vacuum degree in the hermetic container

after sealing.

[0268]

In an image display using the display panel shown in Figs. 17 and 18 thus completed, an image is displayed in such a manner that electrons are emitted by applying scanning signals and modulation signals to each cold cathode device (surface conduction electron emission device) from a signal generator shown in the Fig. 30 through the terminals Dx1 to Dxm and Dy1 to Dyn outside the hermetic container, the emitted electron beams are accelerated by applying a high voltage to the metal back 1019 through a high voltage terminal Hv and caused to collide with the fluorescent film 1018, and the differently colored fluorescent substances 1301 (R, G, B in Fig. 23) are excited and caused to emit light. The voltage Va applied to the high voltage terminal Hv was increased slowly within the range from 3 [kV] to 12 [kV] to a threshold voltage at which electric discharge occurred. The voltage Vf applied between the wiring electrodes 1013 and 1014 was 14 [V]. The withstand voltage was judged to be satisfactory as long as a continuous driving is possible for 1 hours or longer when applying a voltage of 8 kV or higher to the high voltage terminal Hv.

[0269]

Under such conditions, withstand voltage was satisfactory in the vicinity of spacer A. And lines of

emission spots, including the spots formed by the electrons emitted from the cold cathode devices 1012 in the vicinity of spacer A, were made in such a manner that they were spaced at regular intervals in a two-dimensional form. And a color image display excellent in visibility and color reproducibility was obtained. This suggests that the installation of spacer A did not generate the disorder of the electric field which would affect the electron orbits.

[0270]

In the panel adopting the spacers on which a 200 nm thick film of each of GeN, WGeN, SiO_2, CN, and carbon was deposited by sputtering, instead of CrAlN highly resistive film on spacer A, the same effects were obtained.

[0271]

[Example 2] Substrate Material

The metal layer of the substrate surface was subjected to anodic oxidation treatment and sandpaper processing in the same manner as used for the spacer production in example 1 so that the substrate surface would have micro-holes and become rough, except that the master substrate subjected to shape processing was an alumina substrate. In this case, the average diameter and the depth of the opening portions were 100 nm and 500 nm, respectively, and the average roughness of the non-opening portions was 100 nm. Then

a highly resistive film and a low resistive layer were formed by sputtering in the same manner as in example 1. Hereinafter the spacer thus obtained is referred to as spacer B.

[0272]

In the above uneven portion, the coating performance of the film was satisfactory over the boundary regions between the depressed portion and the elevated portion, and the opening regions of the substrate were not filled up by the formation of the highly resistive film. Further, in the non-opening regions, the continuity of the film was satisfactory.

[0273]

The incident angle dependency coefficient of secondary electron emission coefficient m_0 of the spacer B was 2 for the incident electron energy of 1 keV.

[0274]

An electron beam emission apparatus together with a rear plate which incorporated electron beam emission devices in it were produced in the same manner as in example 1, and high voltage application and device driving were performed under the same conditions as in example 1.

[0275]

Under such conditions, withstand voltage was satisfactory in the vicinity of the spacer B. And

lines of emission spots, including the spots formed by the electrons emitted from the cold cathode devices 1012 in the vicinity of the spacer B, were made in such a manner that they were spaced at regular intervals in a two-dimensional form. And a color image display excellent in visibility and color reproducibility was obtained. This suggests that the installation of the spacer B did not generate the disorder of the electric field which would affect the electron orbits.

[0276]

[Example 3] Photolithograph, Wall Structure

A spacer C with a highly resistive film was produced in the same manner as in example 1, except that a selective perforating processing by the photolithographic method was used as a means for roughing the substrate surface.

[0277]

The method of roughing the substrate surface of the spacer C will be shown below. First, the above spacer substrate g0 was subjected to deposition of OFPR-800 by dipping treatment, as a resist material, made by Tokyo Ohka Kogyo Co., Ltd. and to pre-baking on a hot plate at 90°C for 2 minutes. Then the substrate with resist was exposed to ultraviolet light of 405 nm from the face plate edge side to the highly resistive film portion of the rear plate side using a lattice mask pattern in which the repeating cycle y

changes from 50 μm to 10 μm linearly, as shown in Fig. 10. In this case, the sideways repeating cycle was 50 μm and the exposure time was 4 seconds. After the exposure, the substrate surface was developed with MF CD-2 made by Shipley Far East, rinsed with deionized water and dried. Then it was subjected to post-baking on a hot plate at 140°C for 5 minutes. Then the glass surface was etched using hydrofluoric acid as an corrosive in such a manner that the etching depth became 5 μm, and followed by rinsing with deionized water and drying. Finally, the resist was removed using Resist Strip N321, as a remover, made by Nagase & Co., Ltd., and the substrate was rinsed with deionized water to be dried. A highly resistive film and a low resistive layer were formed on the substrate surface by sputtering in the same manner as in example 1.

[0278]

Fig. 4 shows the surface geometry of the highly resistive film portion of the spacer C thus obtained.

[0279]

In the above uneven portion, the coating performance of the film was satisfactory over the boundary regions between the depressed portion and the elevated portion, and the opening regions of the substrate were not filled up by the formation of the highly resistive film. Further, in the non-opening regions, the continuity of the film was satisfactory.

[0280]

The incident angle dependency coefficient of secondary electron emission coefficient m_0 of the spacer C was 2 for the incident electron energy of 1 keV.

[0281]

An electron beam emission apparatus together with a rear plate which incorporated electron beam emission devices in it were produced in the same manner as in example 1, and high voltage application and device driving were performed under the same conditions as in example 1.

[0282]

Under such conditions, withstand voltage was satisfactory in the vicinity of the spacer C. And lines of emission spots, including the spots formed by the electrons emitted from the cold cathode devices 1012 in the vicinity of the spacer C, were made in such a manner that they were spaced at regular intervals in a two-dimensional form. And a color image display excellent in visibility and color reproducibility was obtained. This suggests that the installation of the spacer C did not generate the disorder of the electric field which would affect the electron orbits.

[0283]

[Example 4] Sandblasting, Wall Structure

A spacer D with a highly resistive film was

produced in the same manner as in example 3, except that a selective perforating processing by the sandblasting was used as a means for roughing the substrate surface.

[0284]

The method of roughing the substrate surface of the spacer D will be shown below. First, the above spacer substrate g0 was subjected to sandblasting from the face plate edge side to the highly resistive film portion of the rear plate side using a lattice mask pattern in which the repeating cycle y changes from 50 μm to 10 μm linearly, as shown in Fig. 10. In this case, the sideways repeating cycle was 50 μm. The sandblasting was performed in such a manner that the depths of the opening became 3 μm laterally and 4 μm longitudinally. A highly resistive film and a low resistive layer were formed on the substrate surface by sputtering in the same manner as in example 1.

[0285]

Fig. 5 shows the surface geometry of the highly resistive film portion of the spacer D thus obtained.

[0286]

In the above uneven portion, the coating performance of the film was satisfactory over the boundary regions between the depressed portion and the elevated portion, and the opening regions of the substrate were not filled up by the formation of the

highly resistive film. Further, in the non-opening regions, the continuity of the film was satisfactory.

[0287]

The incident angle dependency coefficient of secondary electron emission coefficient m_0 of the spacer D was 3 for the incident electron energy of 1 keV.

[0288]

An electron beam emission apparatus together with a rear plate which incorporated electron beam emission devices in it were produced in the same manner as in example 1, and high voltage application and device driving were performed under the same conditions as in example 1.

[0289]

Under such conditions, withstand voltage was satisfactory in the vicinity of the spacer D. And lines of emission spots, including the spots formed by the electrons emitted from the cold cathode devices 1012 in the vicinity of the spacer D, were made in such a manner that they were spaced at regular intervals in a two-dimensional form. And a color image display excellent in visibility and color reproducibility was obtained. This suggests that the installation of the spacer D did not generate the disorder of the electric field which would affect the electron orbits.

[0290]

[Example 5] Roughed Foundation Layer, Unevenness

A spacer E with a highly resistive film was produced in the same manner as in example 1, except that a fine-particle dispersion type film, as a second film, was used between the highly resistive antistatic film and the smooth substrate as a means for roughing the substrate surface.

[0291]

The method of roughing the substrate surface of the spacer E will be shown below. Prior to deposition process, the above spacer substrate g0 was subjected to first ultrasonic cleaning in deionized water, isopropyl alcohol (IPA) and acetone for 3 minutes, then drying at 80°C for 30 minutes, and followed by UV ozone cleaning so as to remove organic residues on the surface of the substrate. Then, the substrate surface was subjected to dipping treatment in PAM606EP solution, which is a fine-particle dispersion type highly resistive film made by Catalysts & Chemicals Ind. Co., Ltd., and to heating and firing in an oven at 270°C. This roughing was performed in such a manner that the average particle diameter became 450 Å and the film thickness became 200 Å at the base portion of the binder.

[0292]

A highly resistive film and a low resistive layer were formed on the substrate surface by sputtering in the same manner as in example 1.

[0293]

Fig. 9 shows the surface geometry of the highly resistive film portion of the spacer E thus obtained.

[0294]

The thickness of the highly resistive film was large for the unevenness of the substrate thus obtained, the highly resistive film, however, had unevenness of about 300 Å on its surface following the unevenness of the underlying layer. In the above uneven portion, the coating performance of the film was satisfactory over the boundary regions between the depressed portion and the elevated portion.

[0295]

The incident angle dependency coefficient of secondary electron emission coefficient m_0 of the spacer E was 4 for the incident electron energy of 1 keV.

[0296]

An electron beam emission apparatus together with a rear plate which incorporated electron beam emission devices in it were produced in the same manner as in example 1, and high voltage application and device driving were performed under the same conditions as in example 1.

[0297]

Under such conditions, withstand voltage was satisfactory in the vicinity of the spacer E. And

lines of emission spots, including the spots formed by the electrons emitted from the cold cathode devices 1012 in the vicinity of the spacer E, were made in such a manner that they were spaced at regular intervals in a two-dimensional form. And a color image display excellent in visibility and color reproducibility was obtained. This suggests that the installation of the spacer E did not generate the disorder of the electric field which would affect the electron orbits.

[0298]

[Comparative Example] Planar Spacer

A highly resistive film and a low resistive layer were formed on a substrate surface by sputtering in the same manner as in example 1, except that the smooth substrate g0 was used as it was as a substrate for a spacer without applying the surface roughing processing. Hereinafter the spacer thus obtained is referred to as spacer F. Fig. 11 shows the surface geometry of the highly resistive film portion of the spacer F.

[0299]

The continuity of the film was satisfactory on the highly resistive film portion, unevenness was, however, not formed on that portion.

[0300]

The incident angle dependency coefficient of secondary electron emission coefficient m_0 of the spacer F was 11 for the incident electron energy of 1

keV.

[0301]

An electron beam emission apparatus together with a rears plate which incorporated electron beam emission devices in it were produced in the same manner as in example 1, and high voltage application and device driving were performed under the same conditions as in example 1.

[0302]

Under such conditions, withstand voltage was satisfactory in the vicinity of the spacer F. And an infinitesimal electric discharge was observed, it did not cause the devices to fracture though. In addition, the emission spots caused by the electrons emitted from the cold cathode devices 1012 in the vicinity of spacer F were drawn up to the spacer by a distance of 0.2 times as long as the pitch of a picture device. This suggests that the spacer was electrically charged, and the installation of spacer F generated the disorder of the electric field which would affect the electron orbits.

[0303]

Comparing the surface geometry, incident angle dependency of secondary electron emission coefficient, displacement of emission point and anode withstand voltage of the samples A to E where a lower resistive film of the present invention described above was

formed and the sample F of the comparative example, the electric contact, displacement of emission point and withstand voltage, all of which are panel characteristics, were all satisfactory. Thus spacers with antistatic and highly resistive film suitable for a vacuum- resistant spacer of the electron beam apparatus could be formed. The electric contact used herein means contact of the highly resistive film with the substrate wiring and the face plate wiring via a low resistive film. However, as compared with the comparative example F, the incident angle dependency coefficient of secondary electron emission coefficient of the examples A to E decreased by one-half or more. Thus the effect of restricting the electric charge due to the electrons entering the spacer at an angle was obtained in the examples A to E. In addition, multiple emission phenomenon of secondary electrons was also restricted, thus a spacer having a good beam-stability and high discharge restriction ability was obtained. The treatment for making the surface porous by anodic oxidation, which was used in the example 1, is advantageous in that it makes possible the control of the diameter and the depth of the openings if only the time for the electrolytic treatment is controlled. For example, spending more time in the electrolytic treatment than the example 1 is advantageous in that it changes the shape of the projection portions as shown

in Figs. 7 and 8.

[0304]

[Effect of the Invention]

In accordance with the present invention described above, spacers can be provided in which not only the static charge caused by the direct incident electrons from the closest electron source, but the static charge caused by the cumulative generation of electrons reflected from the face plate and of electrons multiply emitted from the edge surface of the spacers due to the anode applied voltage are restricted by the effect of relaxing the incident angle and the effect of suppressing the cumulative incidence and discharge of the secondary electrons.

[0305]

The above spacers make it possible to produce electron beam type image displays with high definition and long-term reliability in which displacement of emission points and creeping discharge both involved with static electricity are restricted.

[0306]

In addition, the spacer described above makes easier the process for materializing the final uneven geometry. And it makes higher the degree of freedom in designing the geometry; for example, the design is possible in which unevenness has distribution in a film surface. These are because the spacer makes possible

the restriction of static electrification described above if only the surface geometry of its substrate is controlled. Further, it does not require big changes in the existing film formation process. Still further it makes higher the degree of freedom in stoichiometrically designing the film materials, because it does not restrict the film materials used very much. Thus the spacer described above is advantageous from the viewpoint of its production.

[Brief Description of the Drawings]

[Fig. 1] Schematic presentations of a spacer in accordance with Embodiment 1 of the present invention and illustrations of the production process thereof. (a) is a schematic view of a spacer substrate embodying the present invention, and (b) is a view illustrating one part of a surface geometry of a spacer substrate embodying the present invention.

[Fig. 2] A view illustrating a surface geometry of another form of a spacer embodying the present invention.

[Fig. 3] A view illustrating a surface geometry of still another form of a spacer embodying the present invention.

[Fig. 4] A view illustrating a surface geometry of still another form of a spacer embodying the present invention.

[Fig. 5] A view illustrating a surface geometry

of still another form of a spacer embodying the present invention.

[Fig. 6] A view illustrating a surface geometry of still another form of a spacer embodying the present invention.

[Fig. 7] A view illustrating a surface geometry of still another form of a spacer embodying the present invention.

[Fig. 8] A view illustrating a surface geometry of still another form of a spacer embodying the present invention.

[Fig. 9] A view illustrating a surface geometry of still another form of a spacer embodying the present invention.

[Fig. 10] Illustrations of an unevenness formation pattern of spacers Embodiments 3 and 4 embodying the present invention.

[Fig. 11] A view illustrating a surface geometry of a spacer of Comparative Example.

[Fig. 12] A schematic diagram showing a basic model for the calculation of charged electric potential considering the effects of secondary electron emission.

[Fig. 13] A schematic presentation of one example of the relationship between charged voltage and driving time illustrating the accumulation effects of electrification.

[Fig. 14] An illustration of an incident angle of

primary electrons and a distribution of secondary electron emission.

[Fig. 15] A graph illustrating incident angle θ dependency of secondary electron emission coefficient.

[Fig. 16] Photomicrographs of a scanning electron microscope showing the substrate unevenness dependency of incident angle dependency of the amount of secondary electron emission.

[Fig. 17] A partially cutaway view in perspective of a display panel of an image display embodying the present invention.

[Fig. 18] A sectional view of the display panel of Fig. 8 taken along the line A-A'.

[Fig. 19] (a) is a plan view of the planar surface conduction electron emission device used in the embodiments of the present invention, and (b) is a sectional view of the same.

[Fig. 20] A plan view of the substrate of multiple electron beam sources used in one embodiment of the present invention.

[Fig. 21] A sectional view of part of the substrate of multiple electron beam sources used in one embodiment of the present invention.

[Fig. 22] Plan views illustrating the arrangement of fluorescent substances on a face plate of a display panel.

[Fig. 23] A plan view illustrating the

arrangement of fluorescent substances on a face plate of a display panel.

[Fig. 24] Sectional views showing the production process of a planar surface conduction electron emission device.

[Fig. 25] A voltage waveform presentation during energization forming processing.

[Fig. 26] (a) is a presentation of a waveform of the voltage applied during energization activation processing, (b) is a presentation of the variation of emitted current Ie with time.

[Fig. 27] A sectional view of the vertical surface conduction electron emission device used in one embodiment of the present invention.

[Fig. 28] Sectional views showing the production process of a vertical surface conduction electron emission device.

[Fig. 29] A graph showing the typical property of the surface conduction electron emission device used in one embodiment of the present invention.

[Fig. 30] A block diagram schematically showing a configuration of a driving circuit of an image display embodying the present invention.

[Fig. 31] A schematic plan view showing a ladder arrangement electron source of one form of the present invention.

[Fig. 32] A perspective view of a planar image

display containing a ladder arrangement electron source of one form of the present invention.

[Fig. 33] A schematic diagram of one example of the conventional surface conduction electron emission device.

[Fig. 34] A schematic diagram of one example of the conventional FE type device.

[Fig. 35] A schematic diagram of one example of the conventional MIM type device.

[Fig. 36] A perspective view of a display panel, partially broken away, of the conventional planar image display.

[Description of Reference Numerals or Symbols]

1 Spacer substrate

3, 21 Low resistive film

5 Side surface

11 Highly resistive film

1011 Substrate

1102, 1103 Device electrode

1104 Conductive thin film

1105 Electron emission portion formed by the energization forming processing

1113 Film formed by the energization activation processing

1015 Rear plate

1016 Side wall

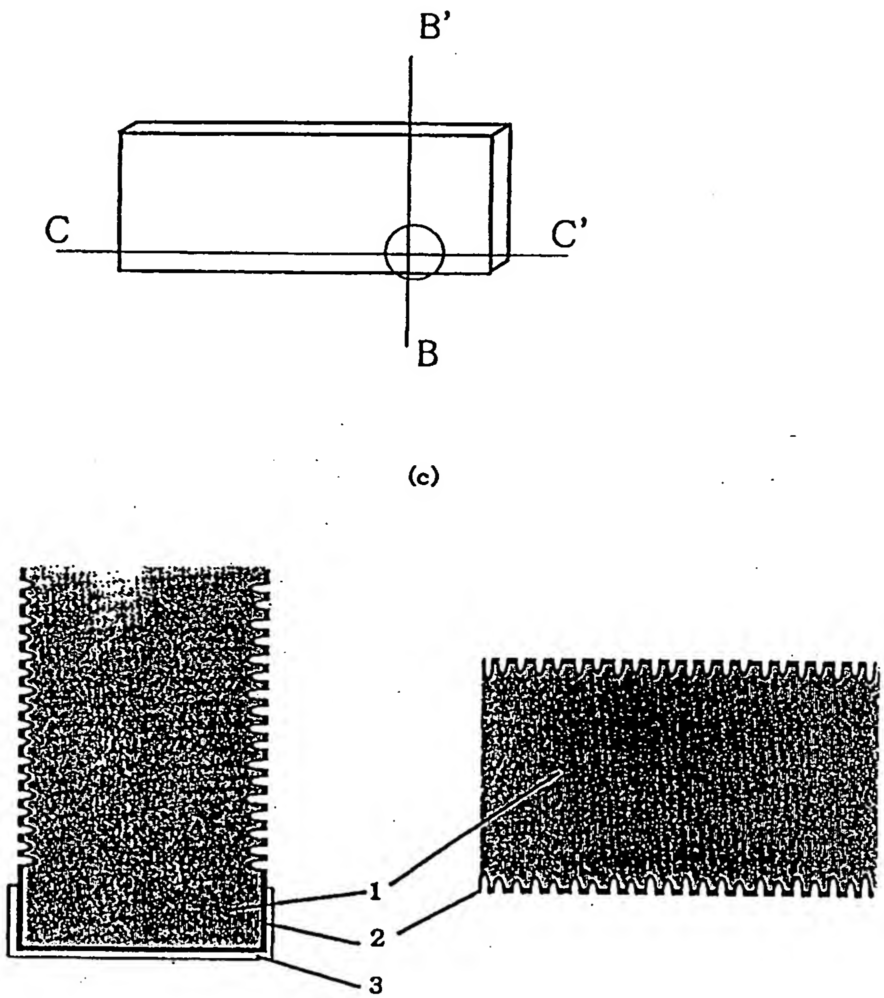
1017 Face plate (FP)

1020 Spacer

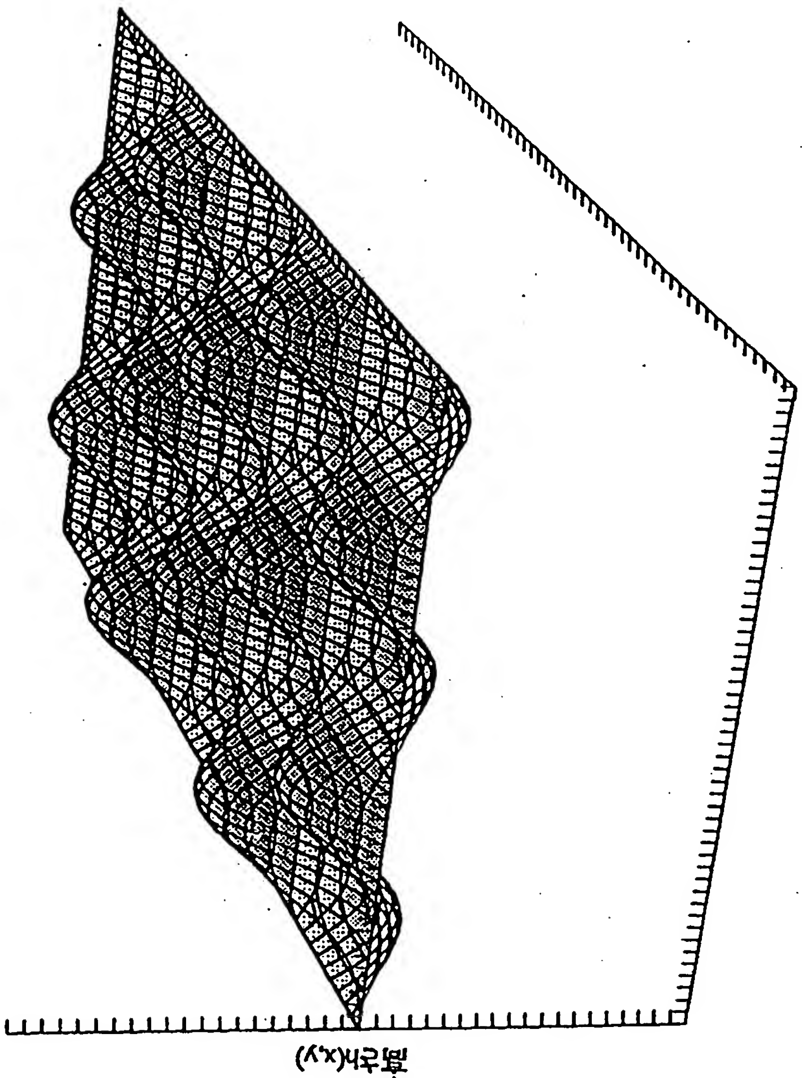
【書類名】　図面　〔Name of the Document〕 Drawings

【図１】 Fig. 1

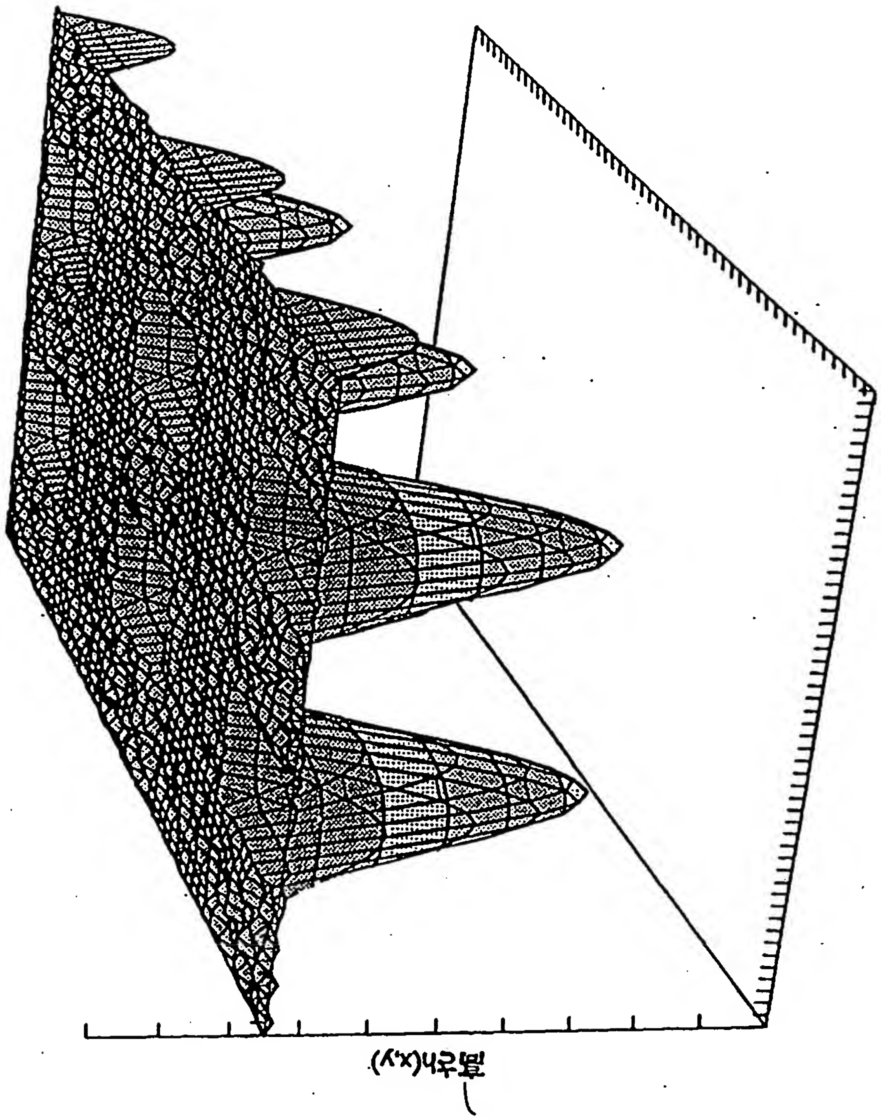
(a)



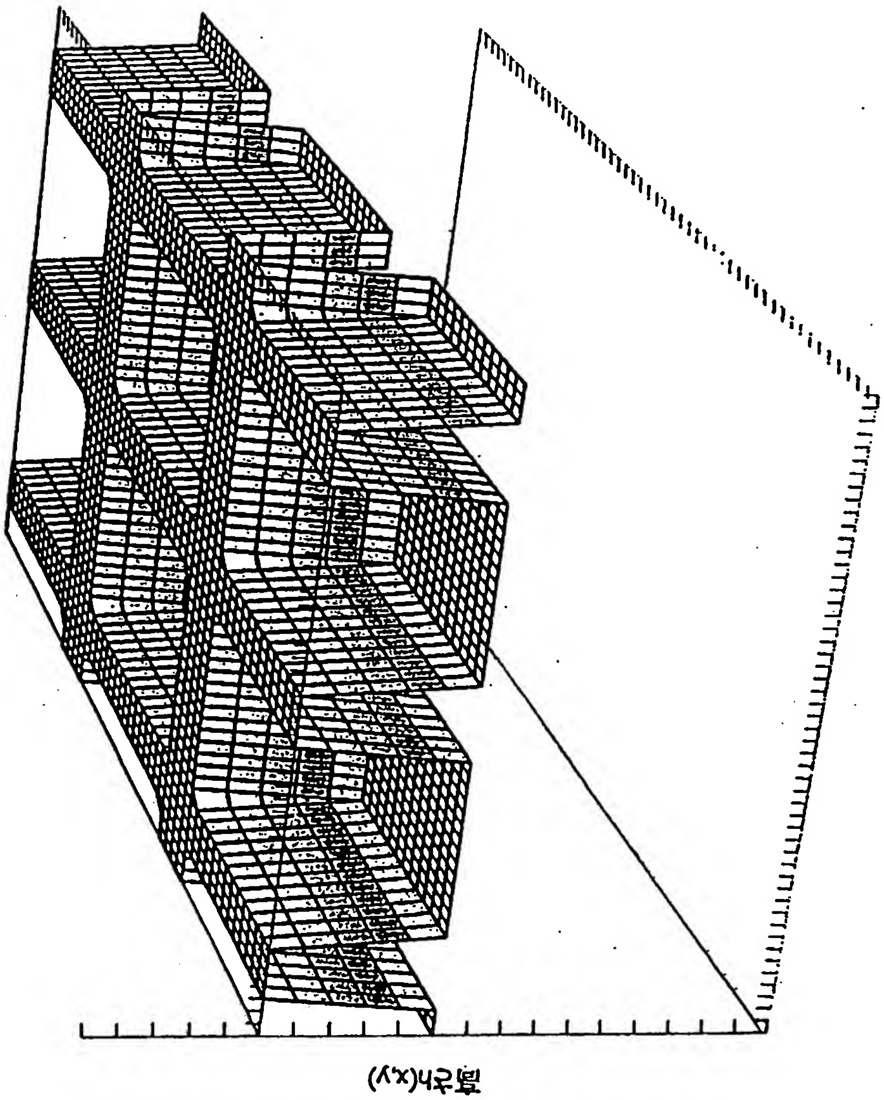
【図２】 Fig. 2



【図３】 Fig. 3

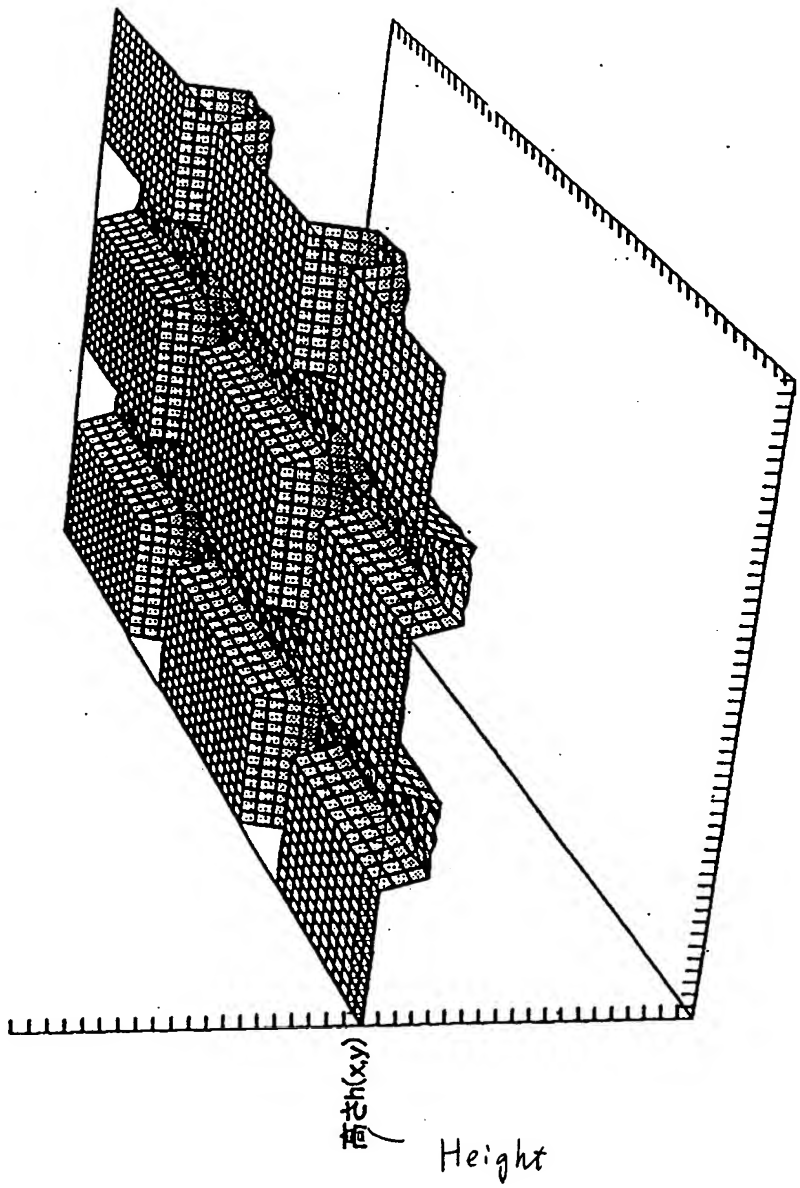


【図４】 Fig. 4

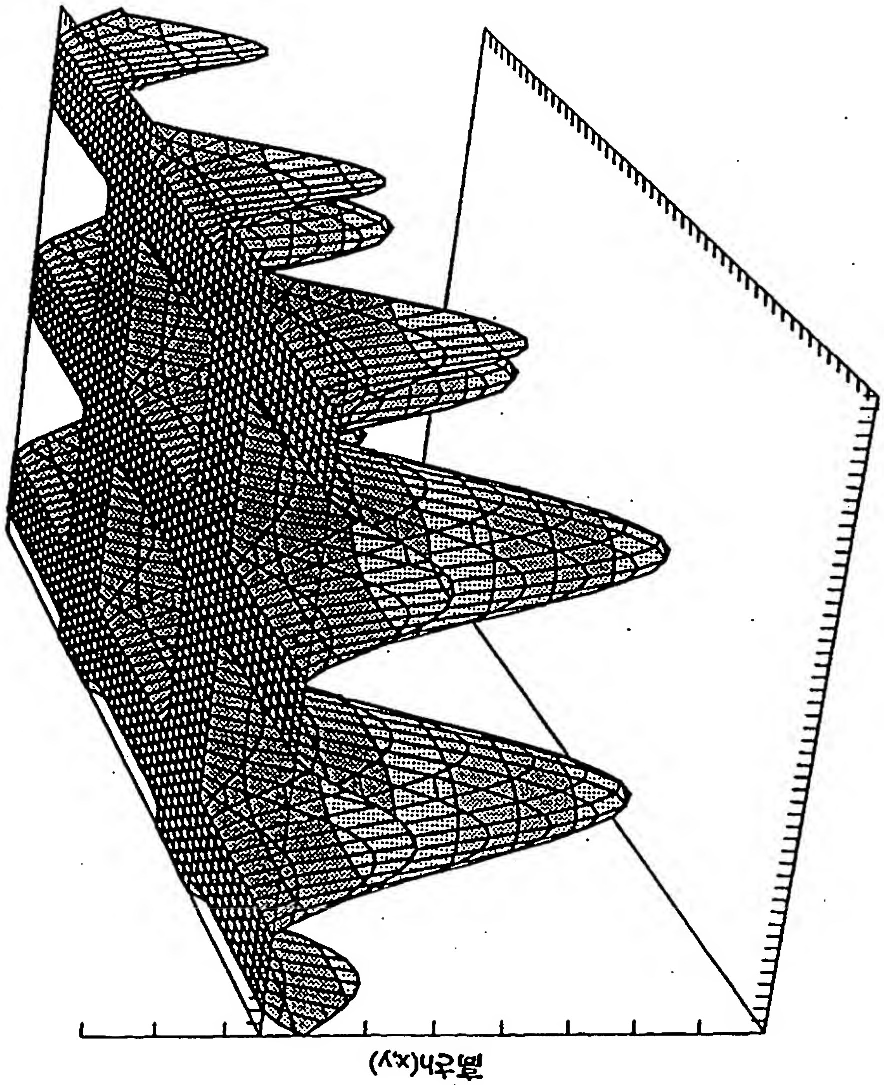


Height

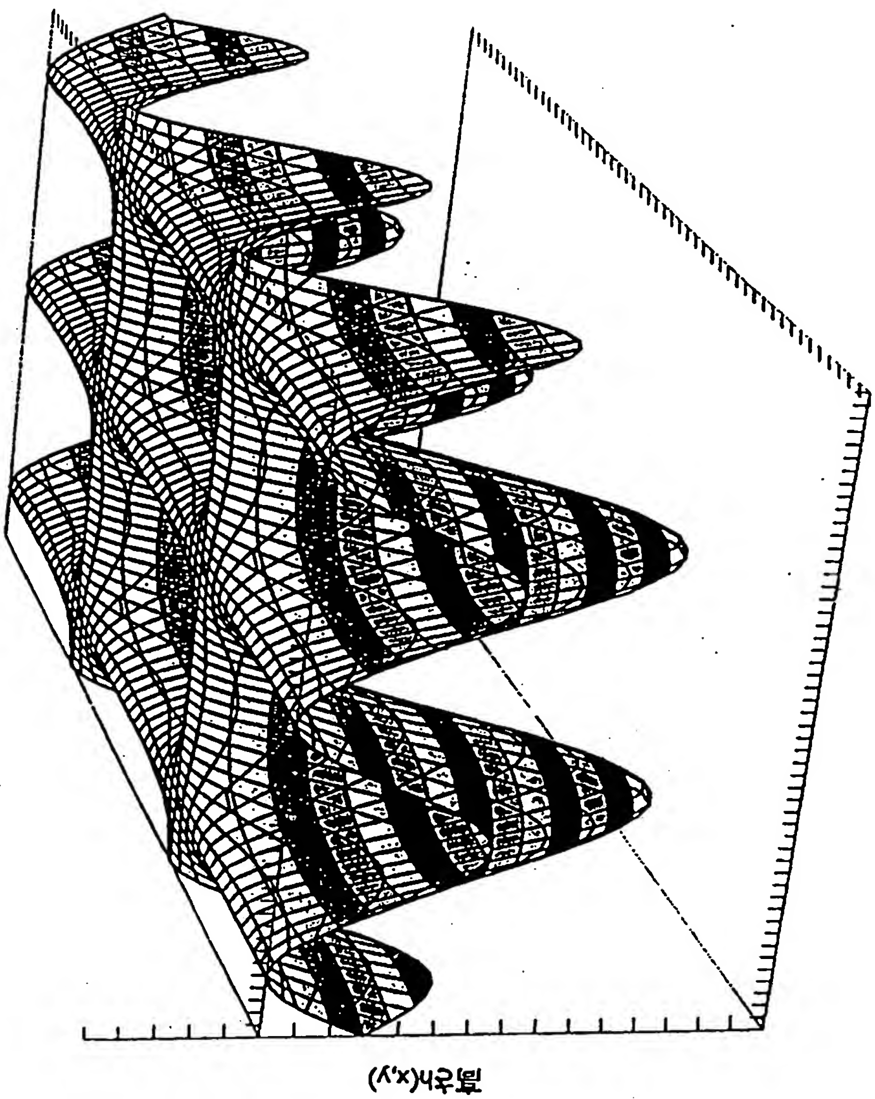
【図５】 Fig. 5



【図６】 Fig. 6

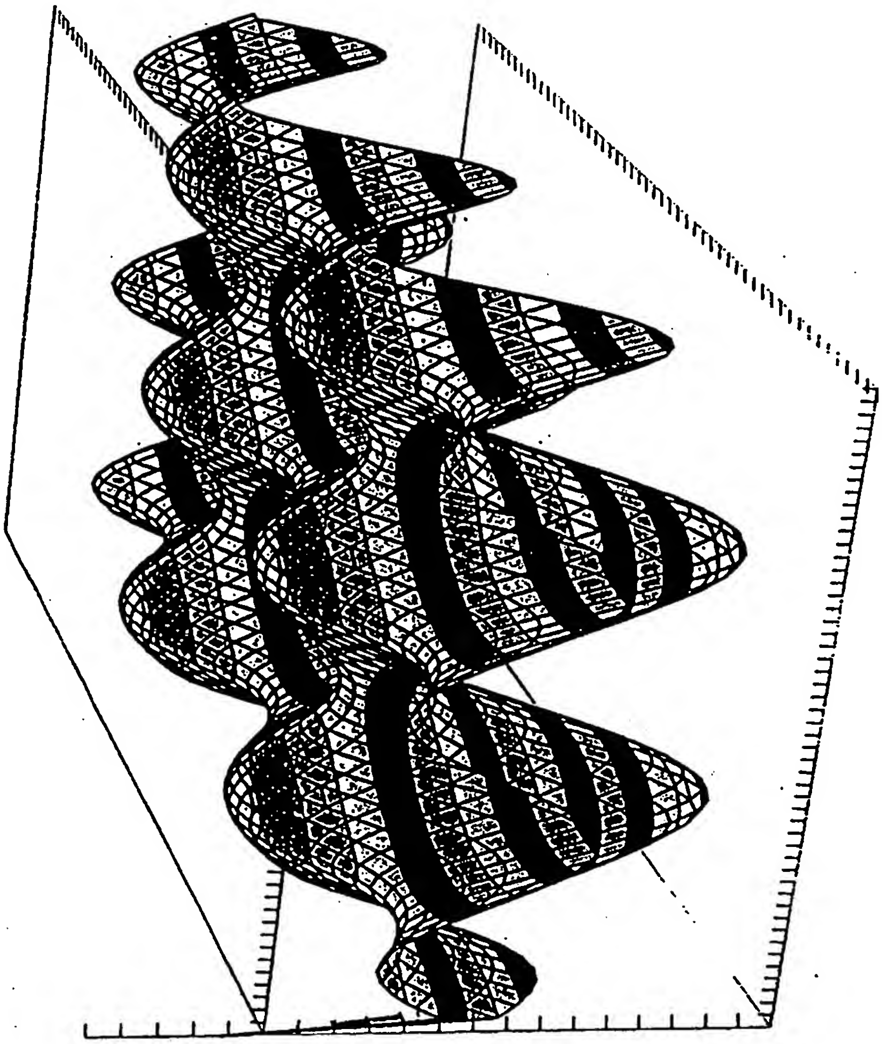


【図７】 Fig. 7

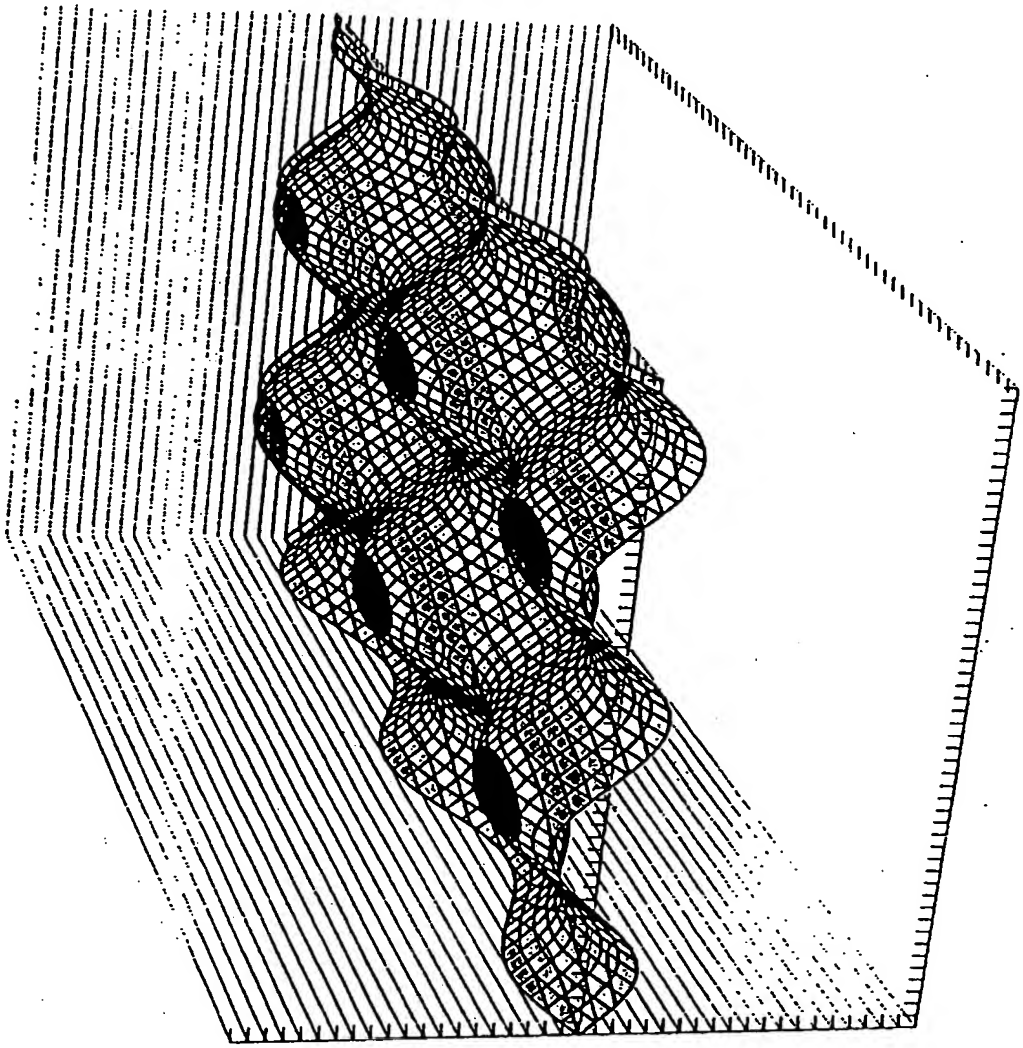


Height

【図８】 Fig. 8



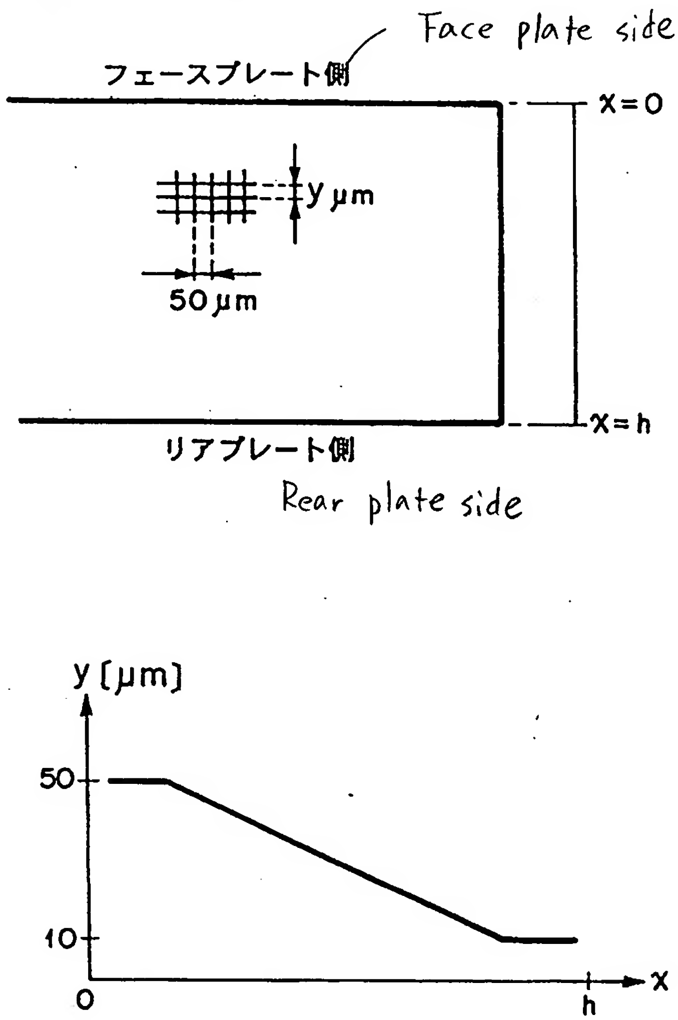
【図９】 Fig. 9



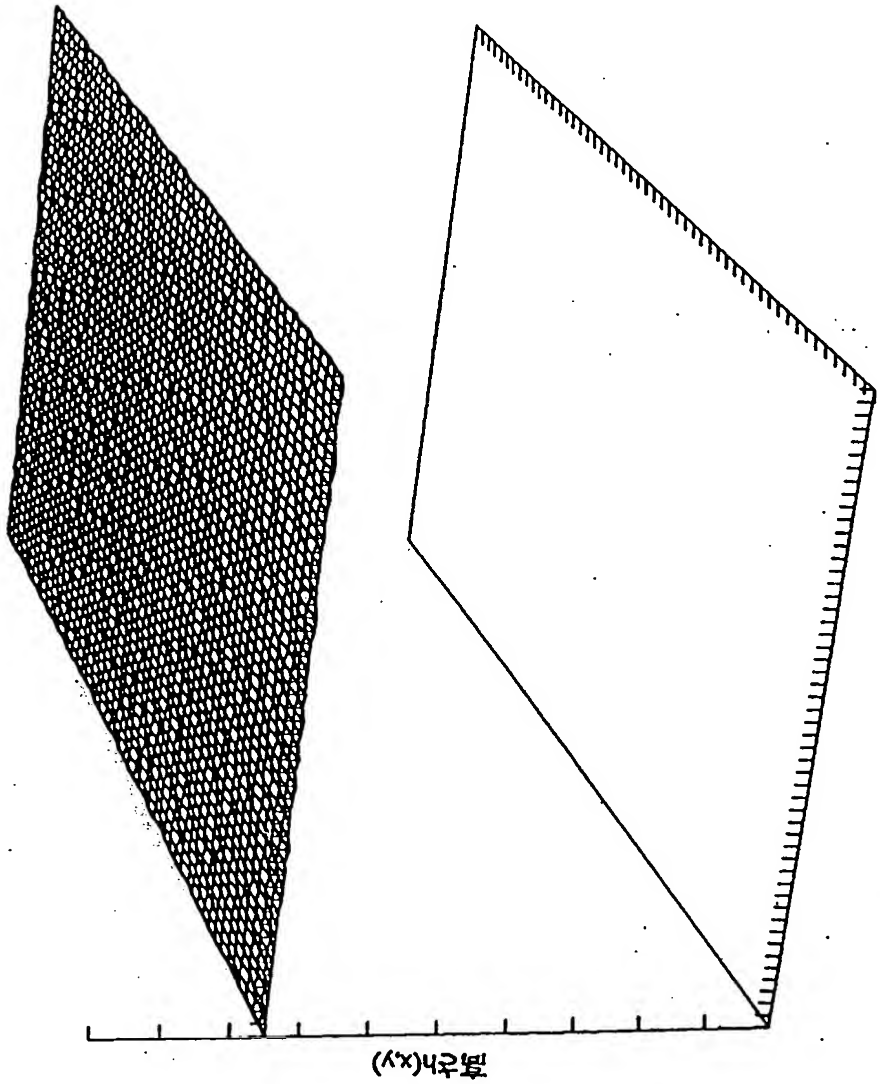
高さh(x,y)

Height

【図１０】 Fig. 10

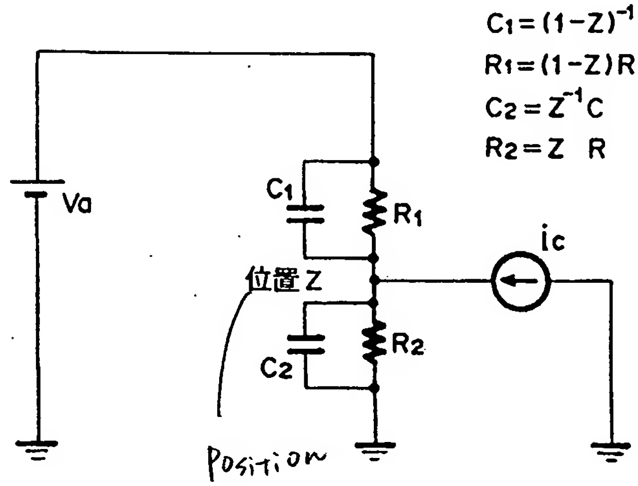

フェースプレート側
Face plate side
x=0
y μm
50μm
x=h
リアプレート側
Rear plate side
y [μm]
50
10
0
h
x

【図１１】 Fig. 11

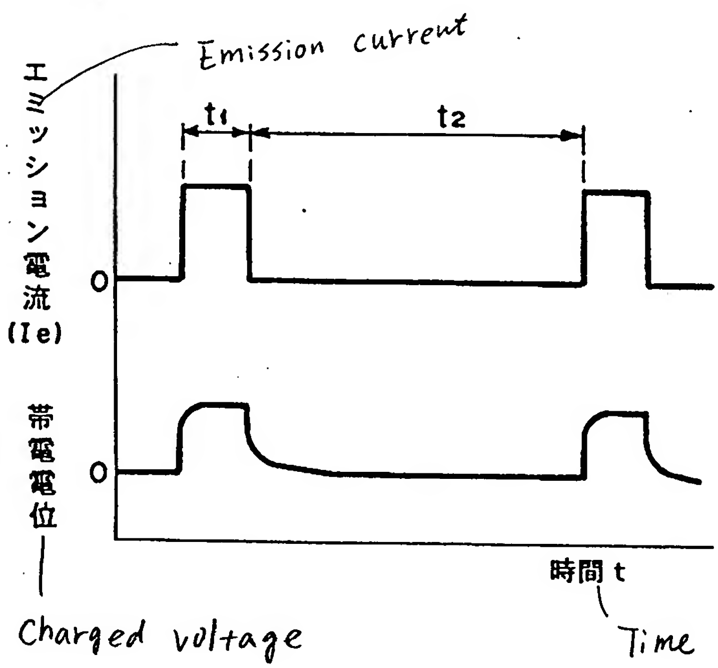


Height

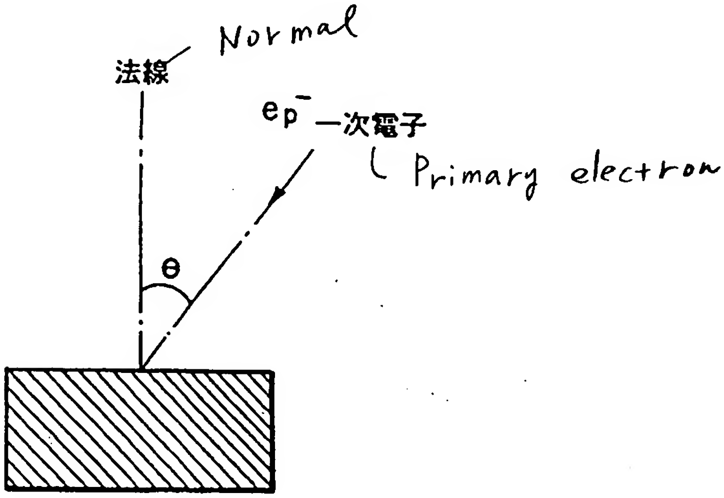
【図１２】 Fig. 12



【図１３】 Fig. 13



【図１４】 Fig. 14

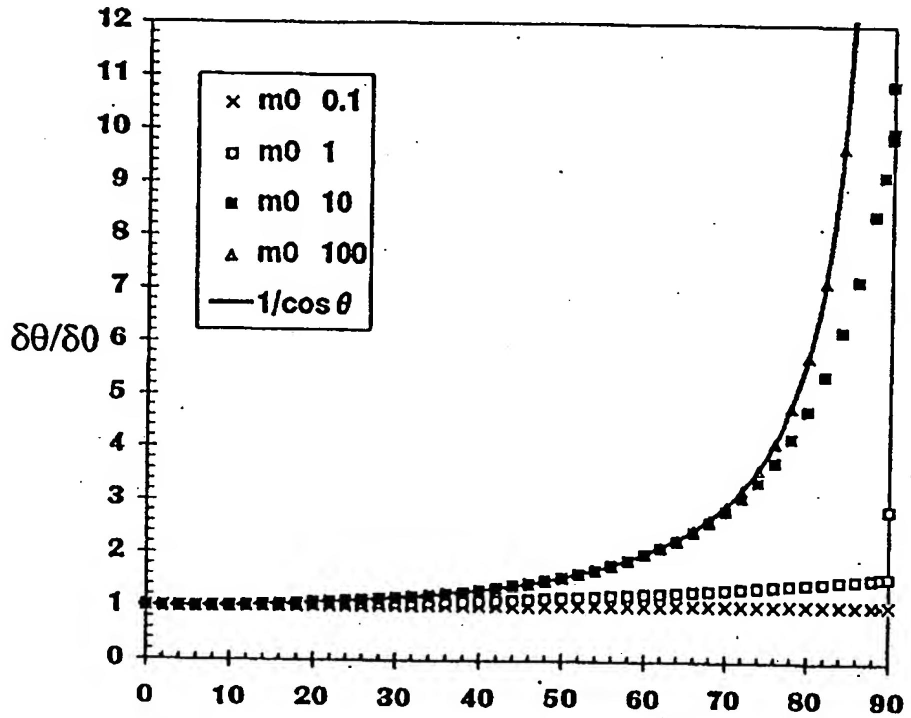


【図１５】 Fig. 15

Incident angle dependency of secondary electron emission coefficient

二次電子放出係数の入射角増依存特性

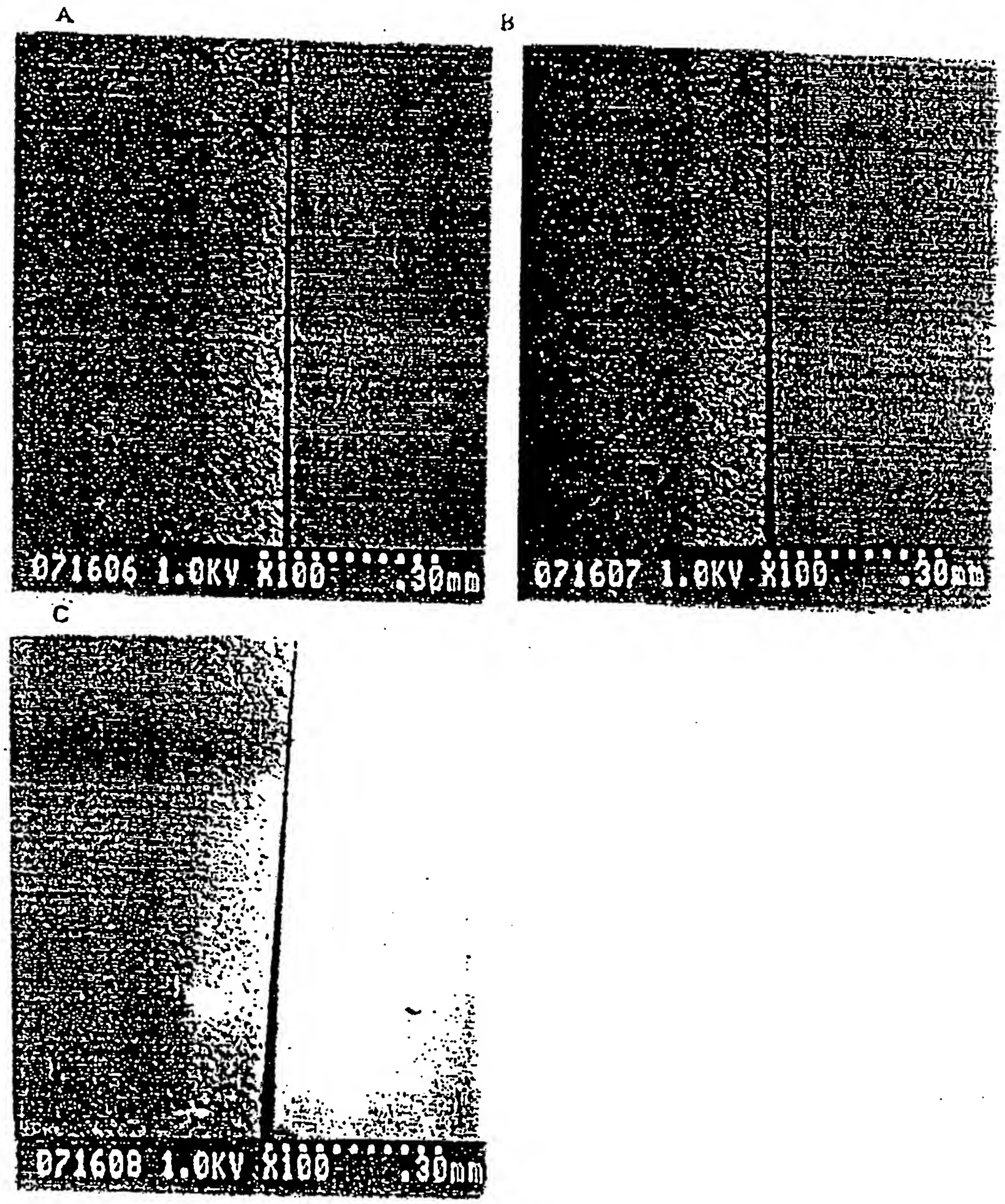
$$\frac{\delta\theta}{\delta 0}=\frac{1}{\cos\theta}\cdot\frac{1-\exp(-m0\times\cos\theta)}{1-\exp(-m0)}$$



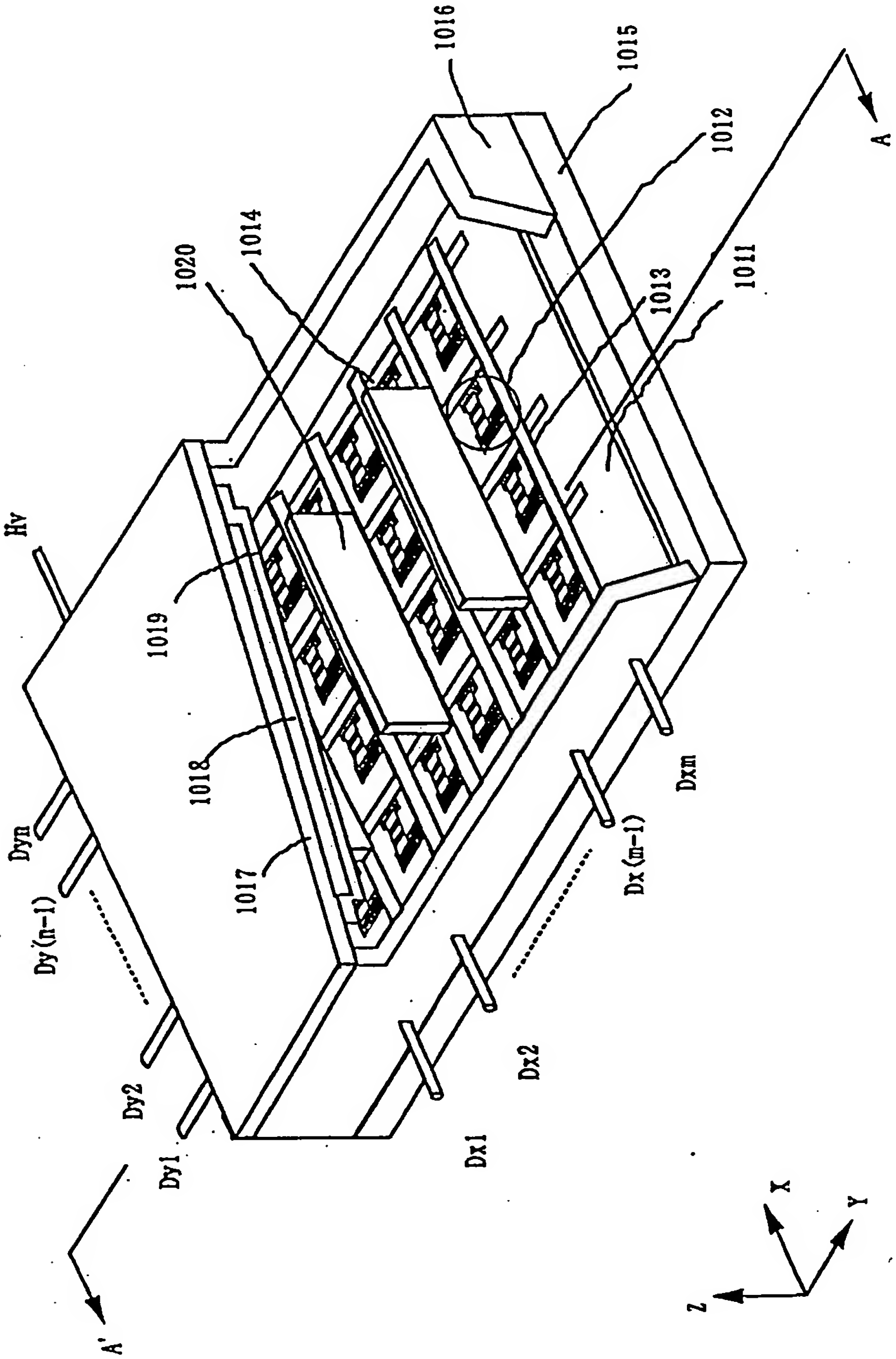
入射角 θ [degree]

Incident angle

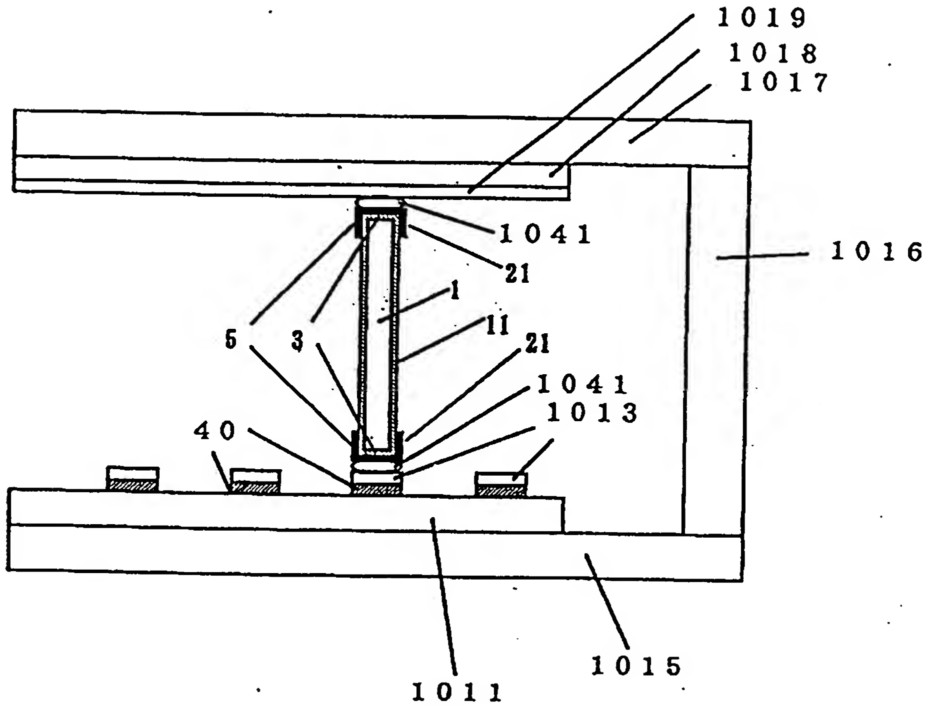
【図１６】 Fig. 16


A
B
C
071606 1.0KV X100 .30mm
071607 1.0KV X100 .30mm
071608 1.0KV X100 .30mm

【図１７】 Fig. 17

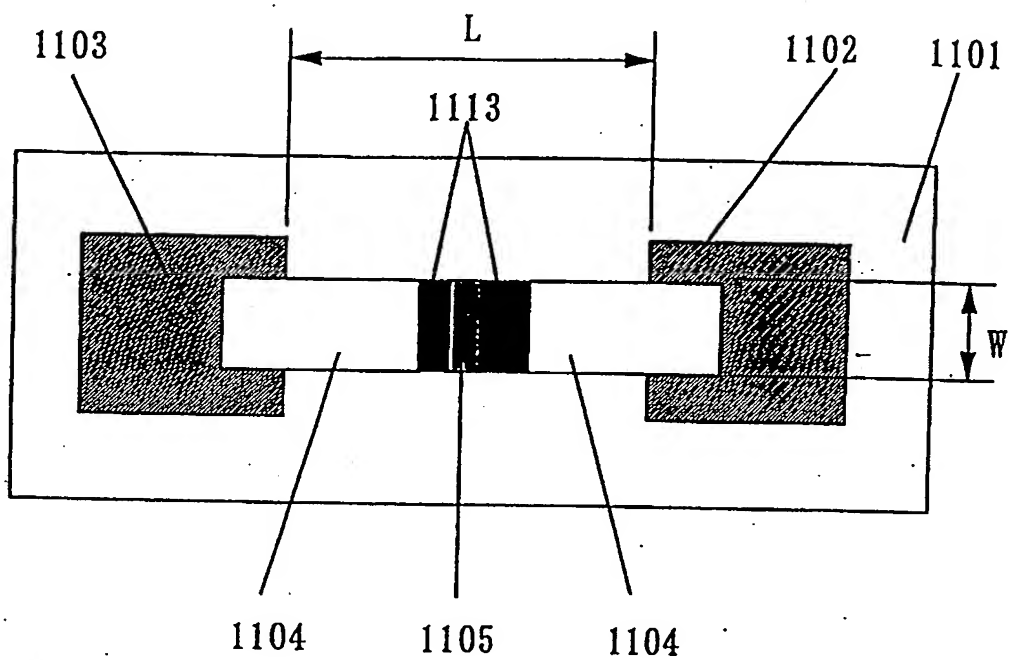

1016
1015
1012
A
1014
1020
1013
1011
Hv
1019
1018
Dyn
Dy(n-1)
1017
Dxm
Dx(m-1)
Dx2
Dy2
Dx1
Dy1
A'
X
Y
Z

【図１８】 Fig. 18

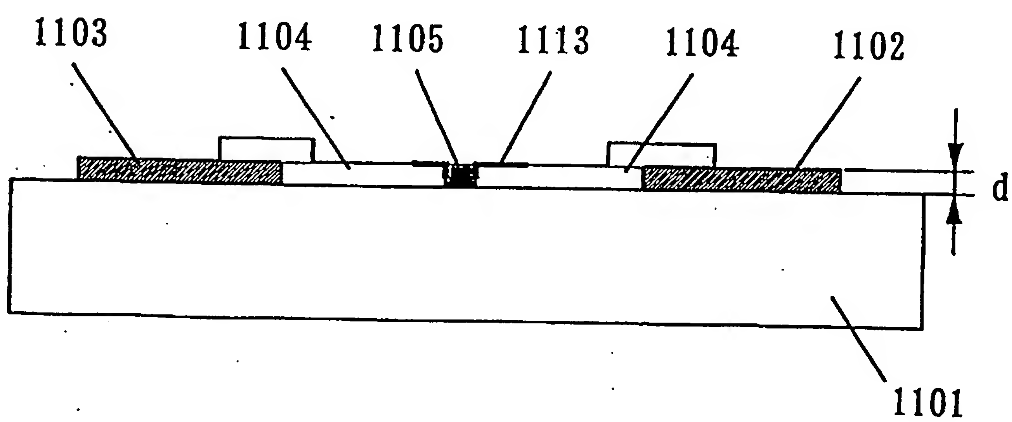


【図１９】 Fig. 19

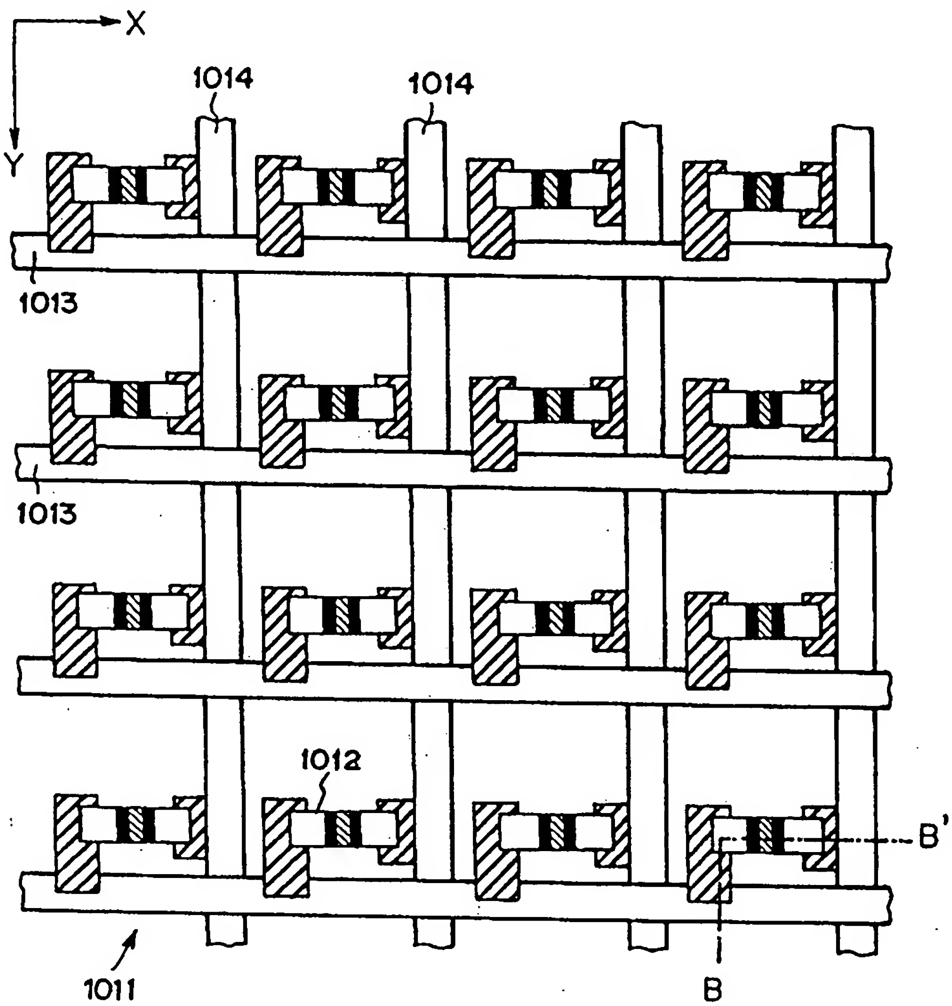
(a)


L
1103
1102
1101
1113
W
1104
1105
1104

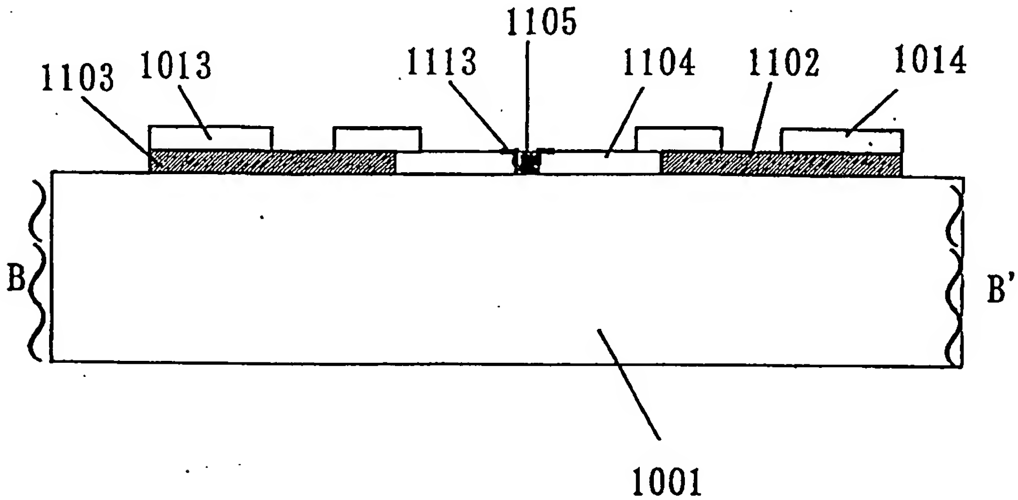
(b)


1103
1104
1105
1113
1104
1102
d
1101

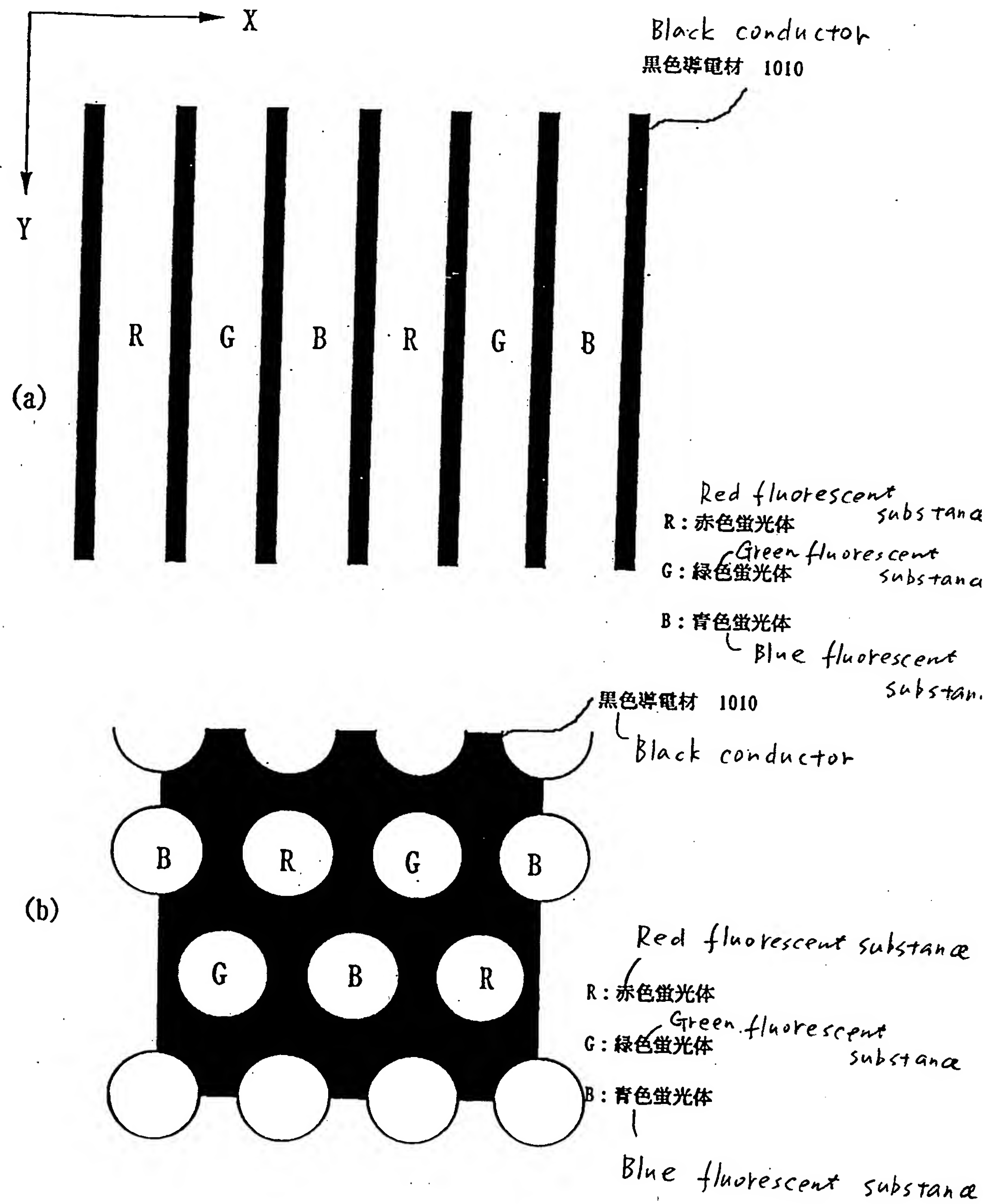
【図２０】 Fig. 20



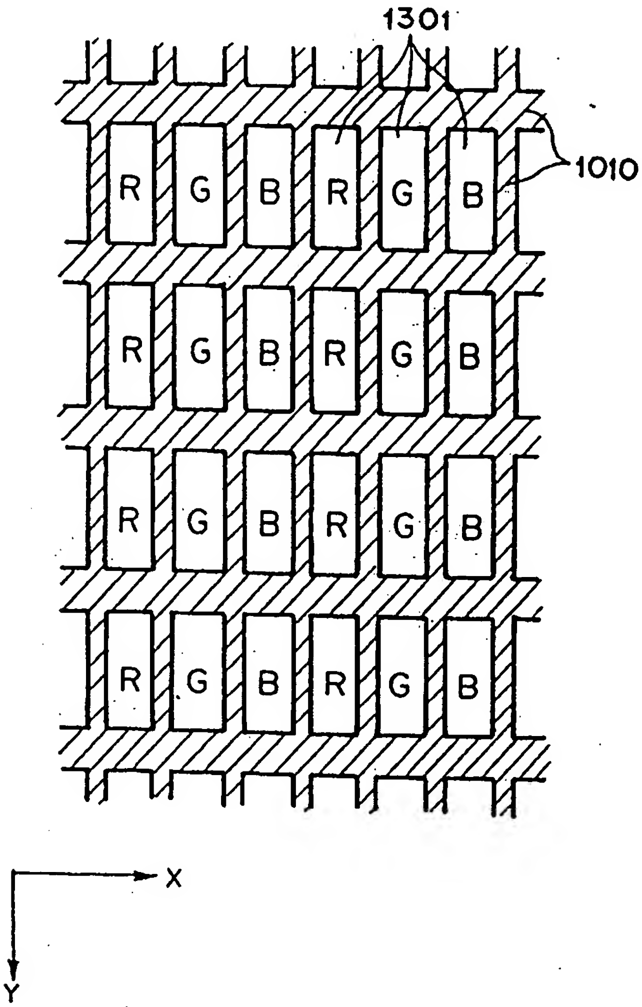
【図２１】 Fig. 21



【図２２】 Fig. 22


X
Y
Black conductor
黒色導電材　1010
R
G
B
R
G
B
(a)
Red fluorescent substance
R：赤色蛍光体
Green fluorescent substance
G：緑色蛍光体
B：青色蛍光体
Blue fluorescent substan.
黒色導電材　1010
Black conductor
B
R
G
B
G
B
R
(b)
Red fluorescent substance
R：赤色蛍光体
Green fluorescent substance
G：緑色蛍光体
B：青色蛍光体
Blue fluorescent substance

【図２３】 Fig. 23



【図２４】　Fig. 24

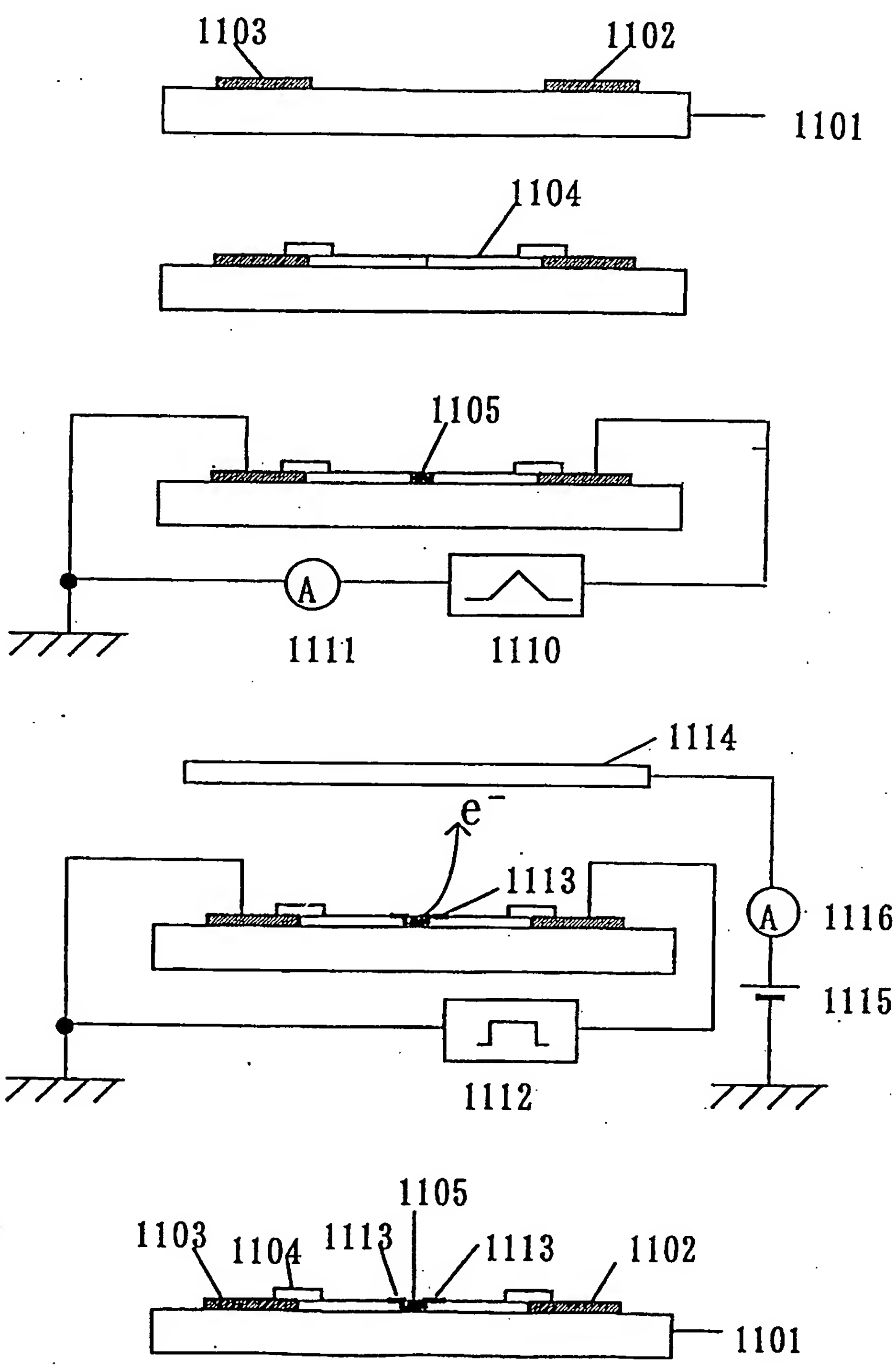
(a)

(b)

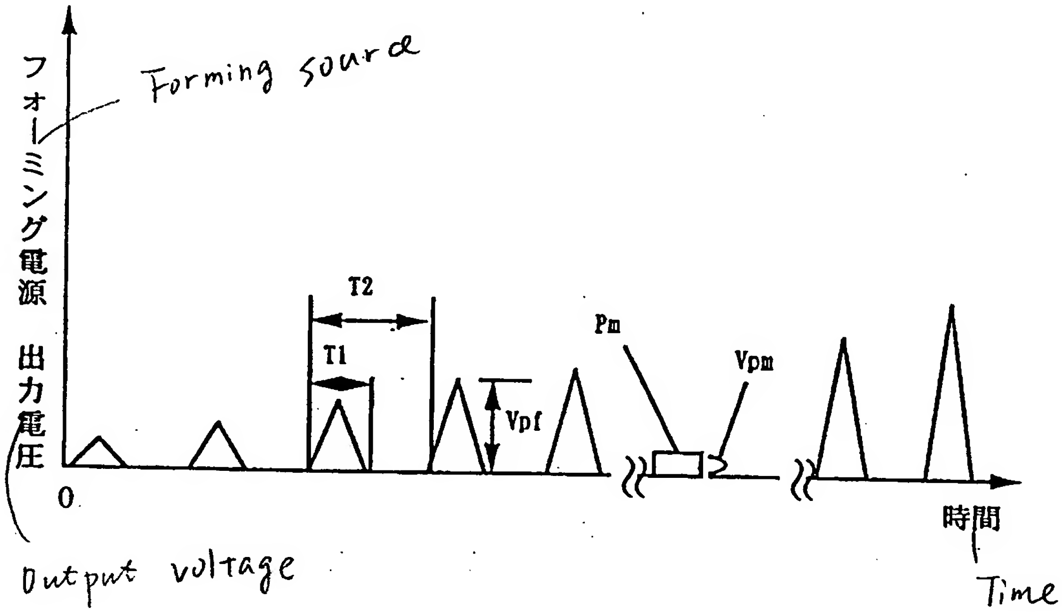
(c)

(d)

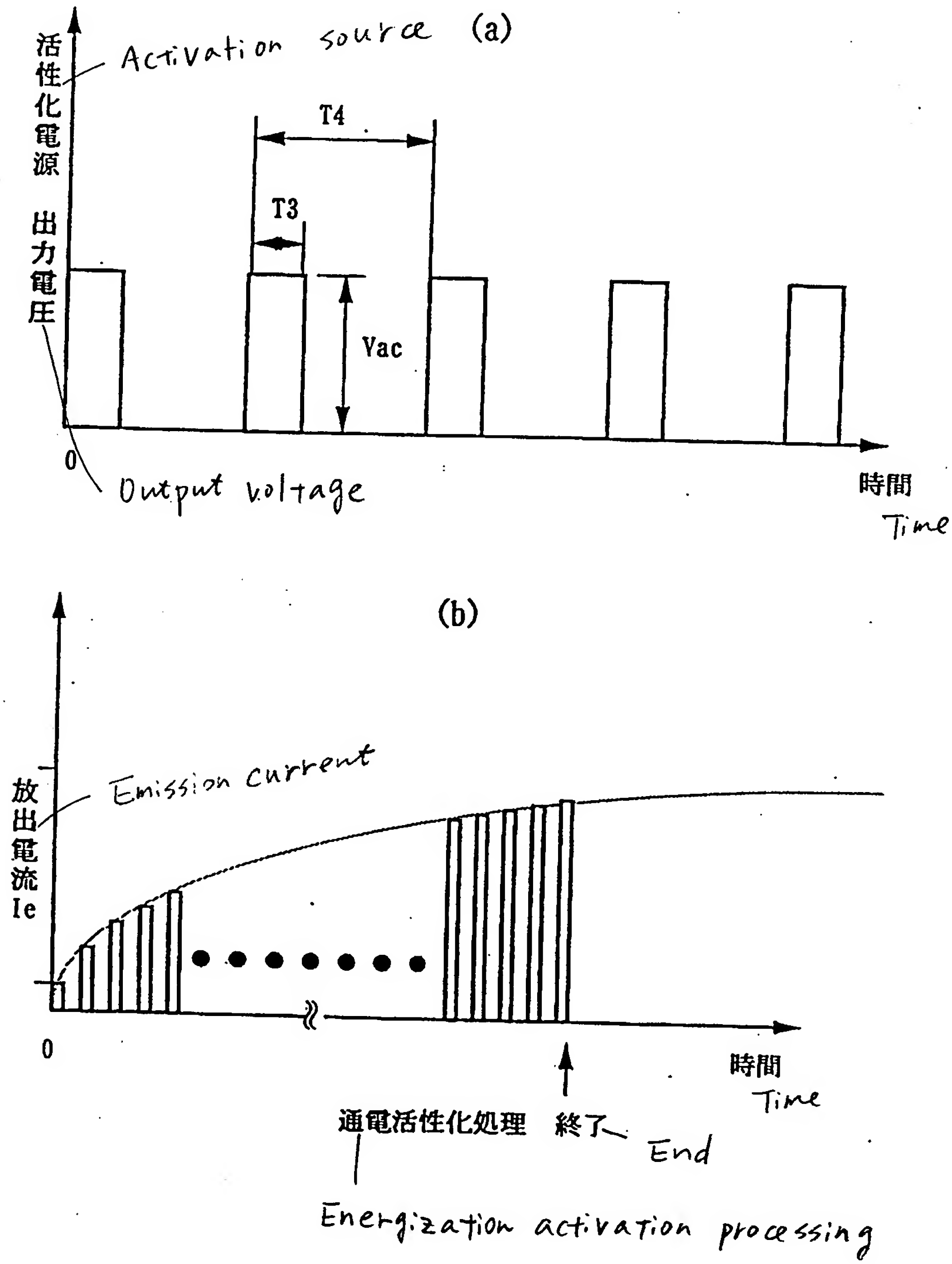
(e)



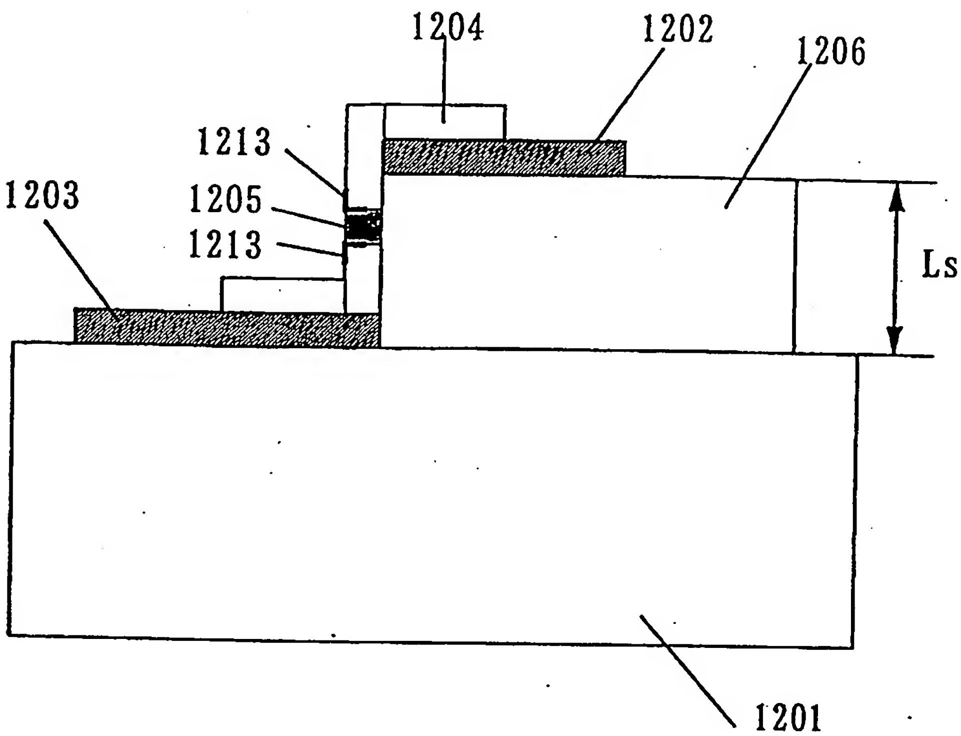
【図２５】 Fig. 25


フォーミング電源 出力電圧
Forming source
Output voltage
T2
T1
Vpf
Pm
Vpm
0
時間
Time

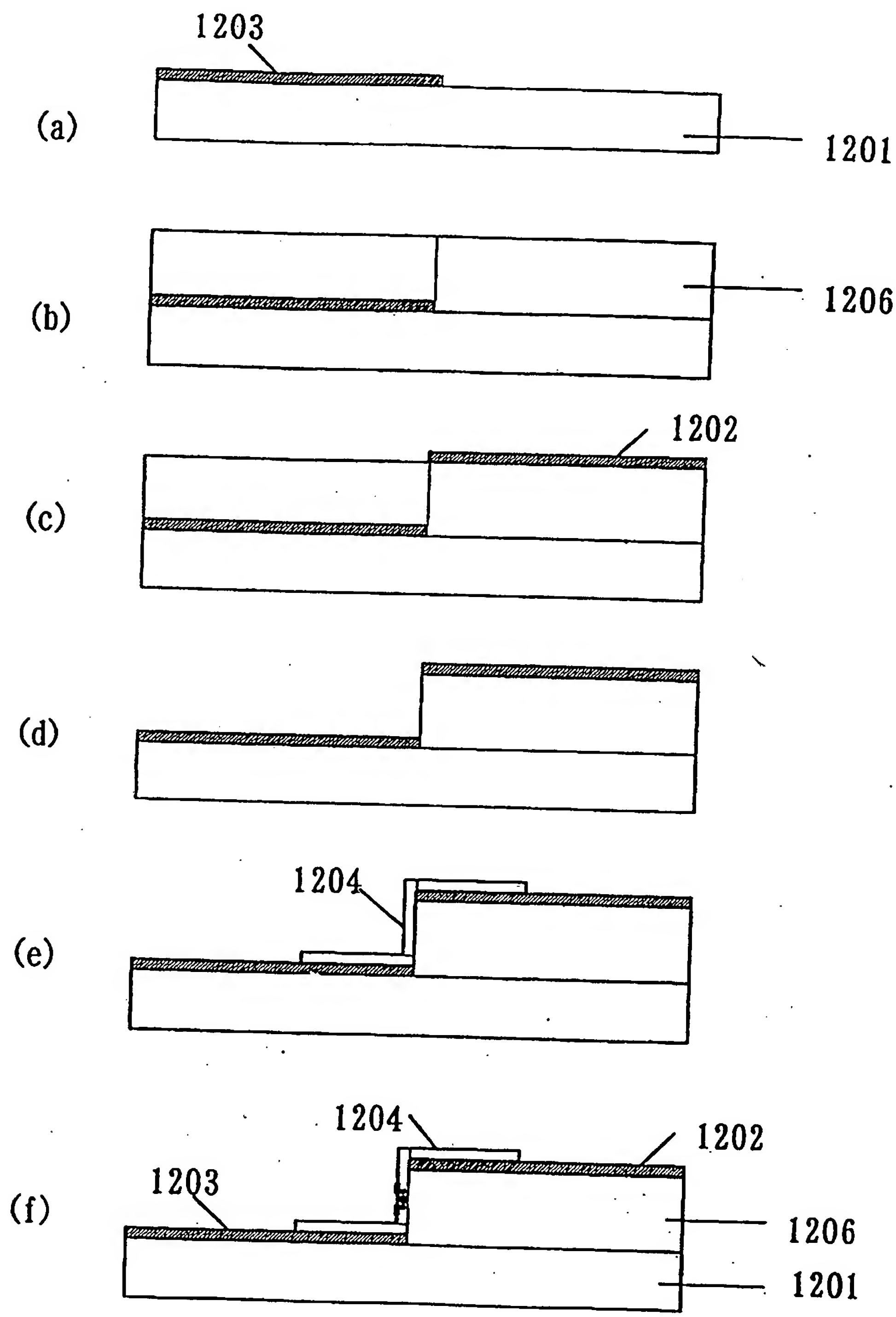
【図２６】 Fig. 26


活性化電源 出力電圧
Activation source
(a)
T4
T3
Vac
0
Output voltage
時間
Time
(b)
放出電流 Ie
Emission current
0
時間
Time
通電活性化処理
終了
End
Energization activation processing

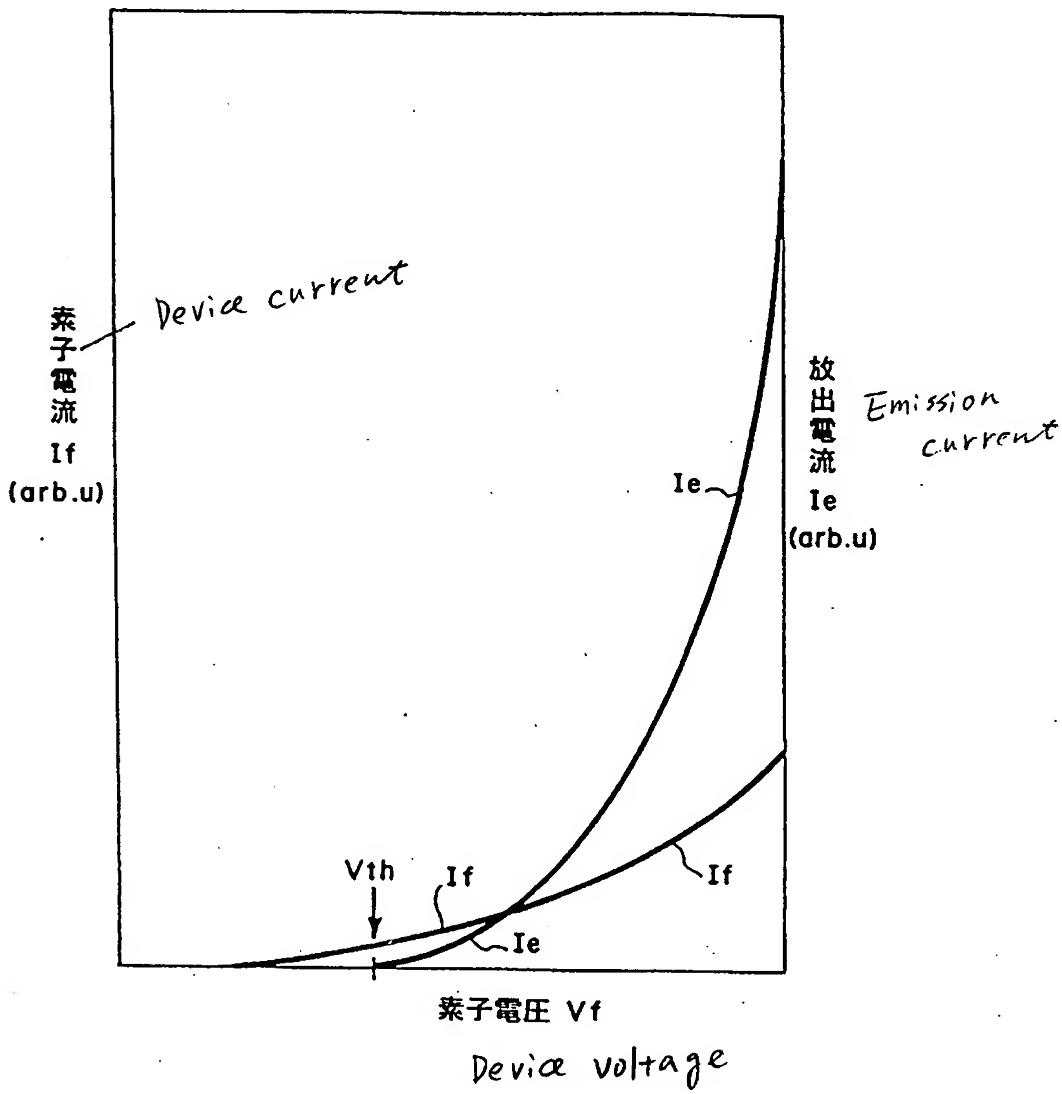
【図２７】 Fig. 27



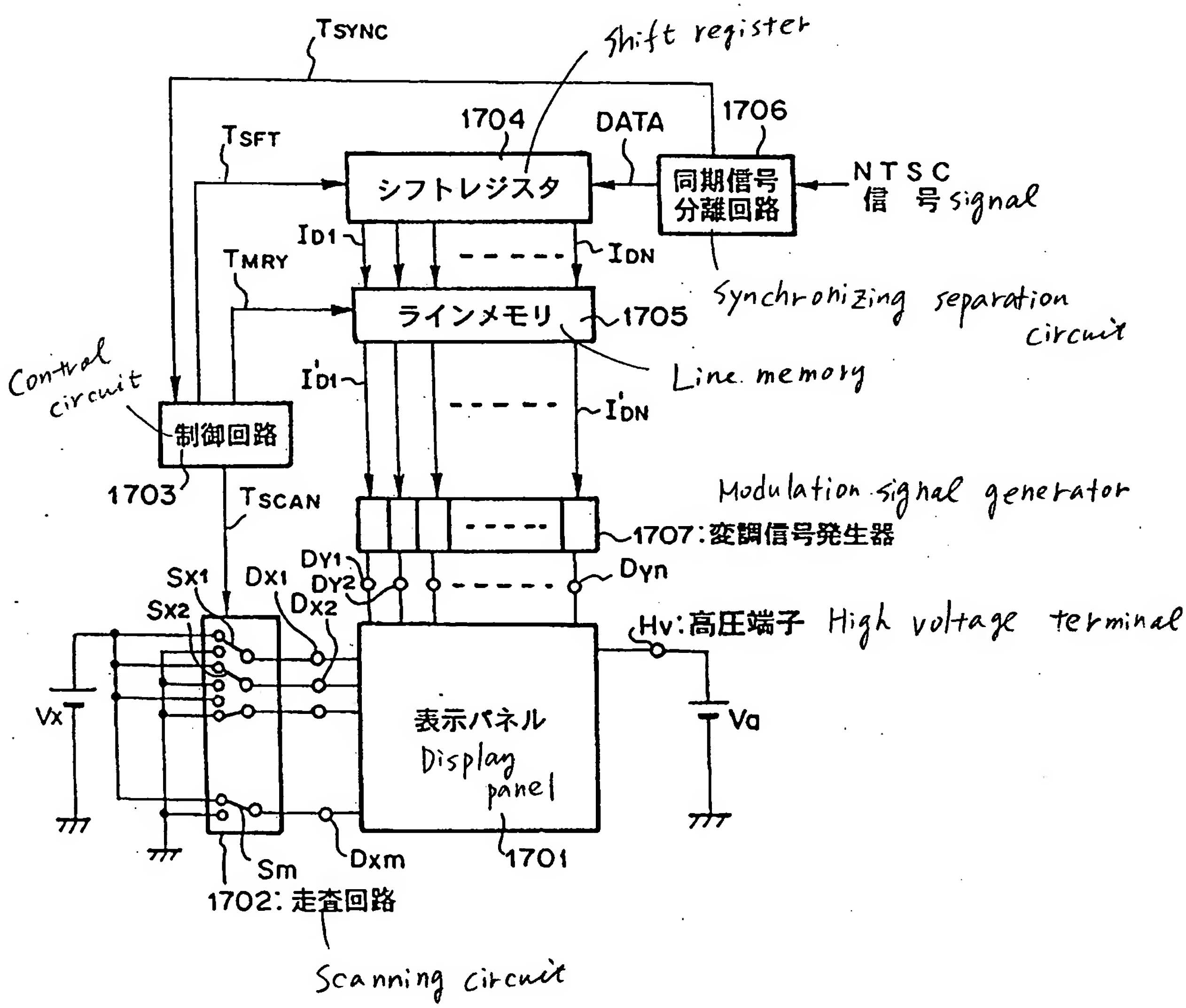
【図２８】 Fig. 28



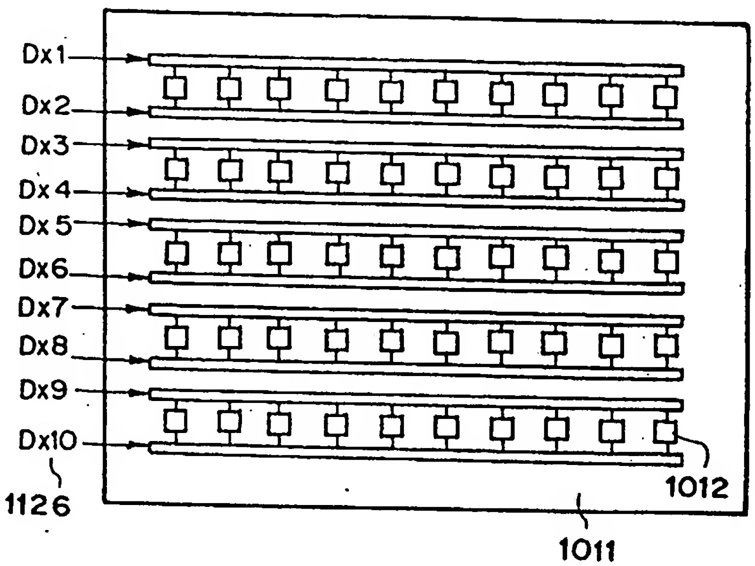
【図２９】 Fig. 29


素子電流
Device current
If
(arb.u)
放出電流
Emission current
Ie
(arb.u)
Ie
Vth
If
If
Ie
素子電圧 Vf
Device voltage

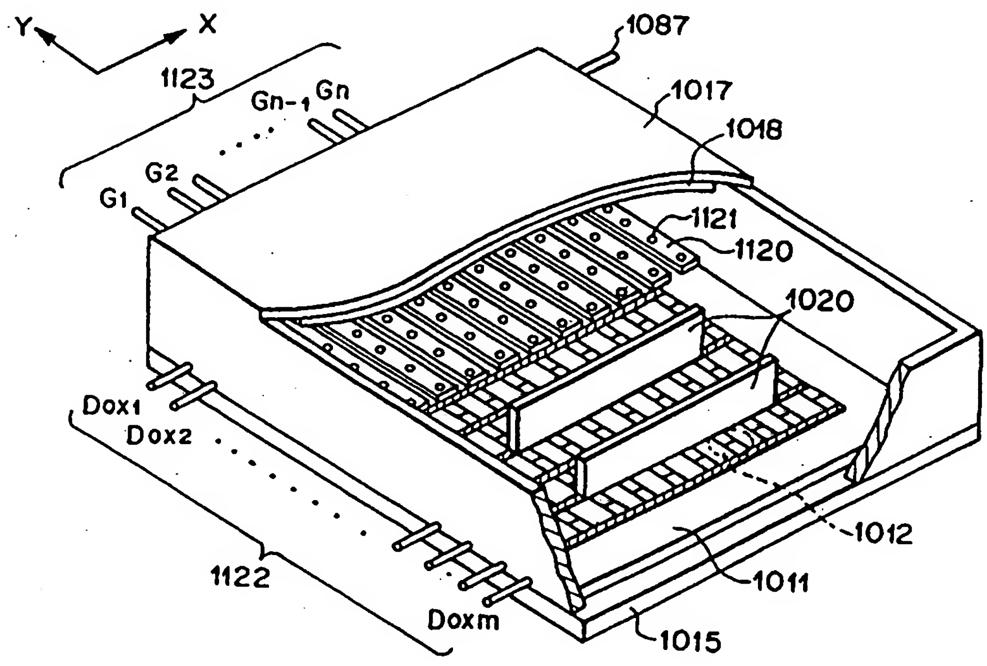
【図３０】 Fig. 30


TSYNC
Shift register
1704
DATA
1706
TSFT
シフトレジスタ
同期信号
分離回路
NTSC
信 号 signal
ID1
IDN
TMRY
ラインメモリ
1705
Synchronizing separation circuit
Control circuit
I'D1
I'DN
Line memory
制御回路
1703
TSCAN
Modulation signal generator
1707:変調信号発生器
DY1
DY2
Dyn
SX1
DX1
SX2
DX2
Hv:高圧端子 High voltage terminal
Vx
Va
表示パネル
Display panel
Sm
Dxm
1701
1702:走査回路
Scanning circuit

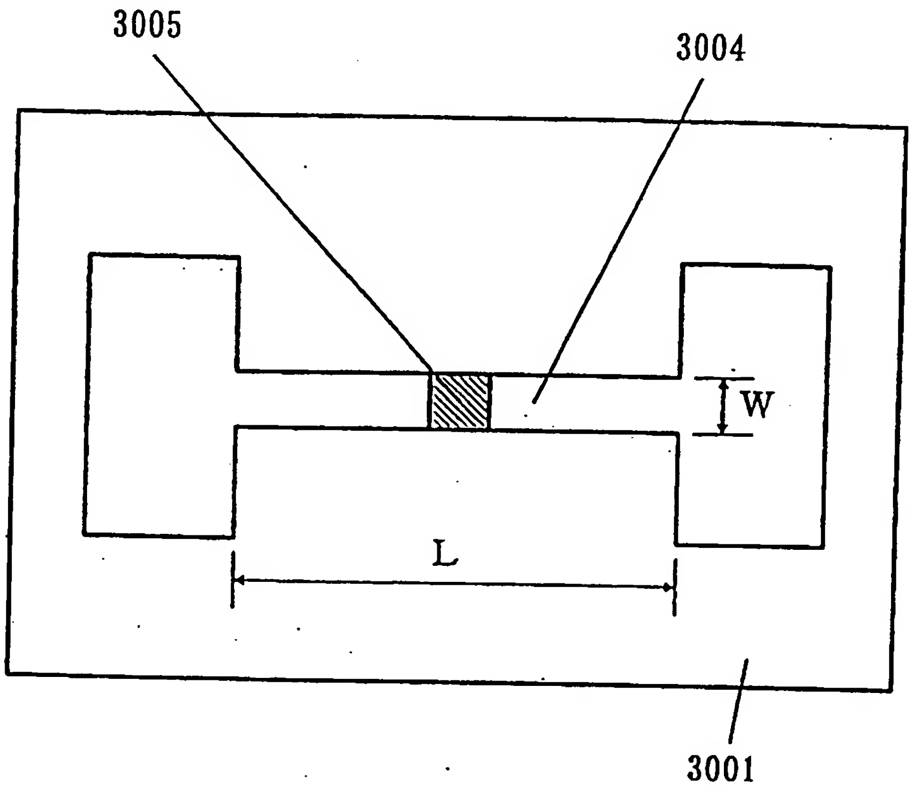
【図３１】 Fig. 31



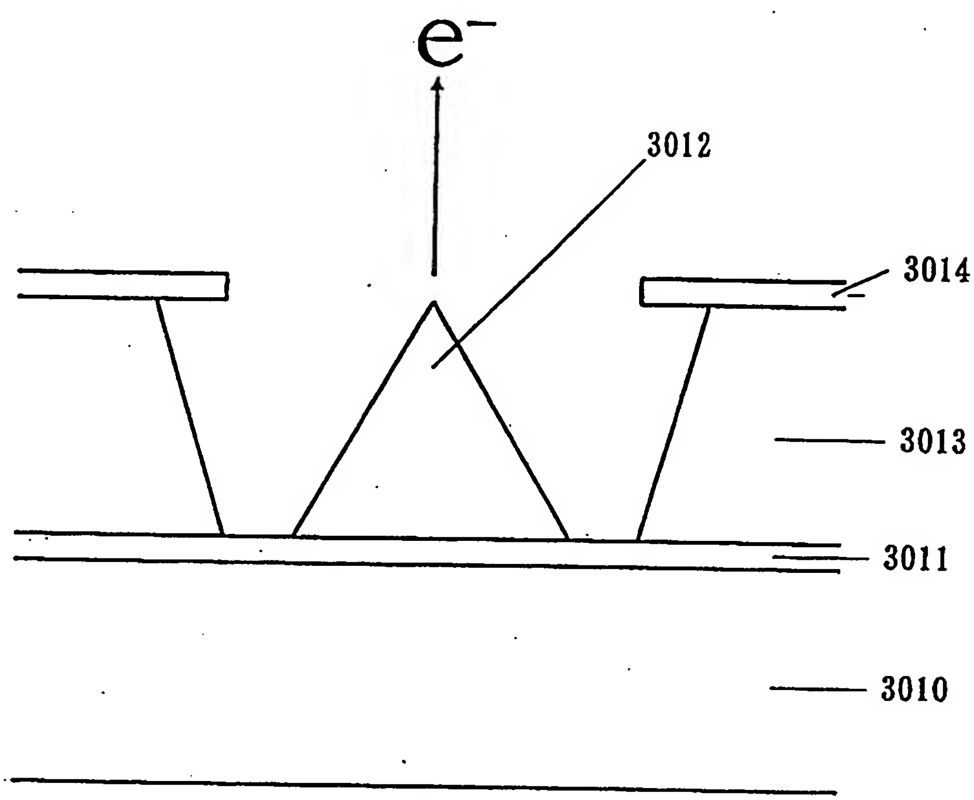
【図３２】 Fig. 32



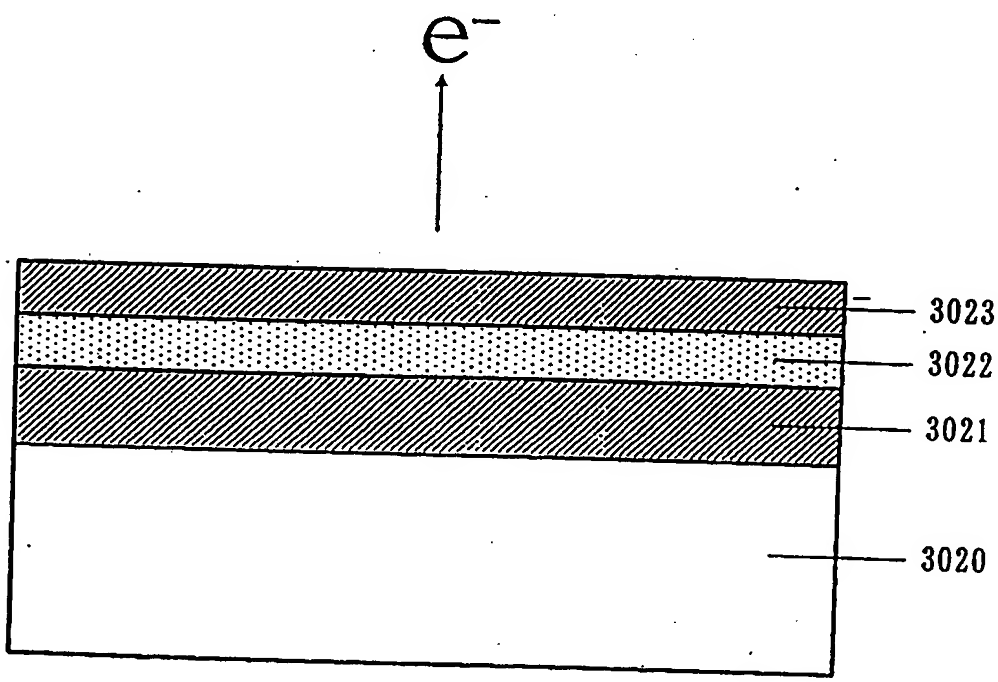
【図３３】 Fig. 33



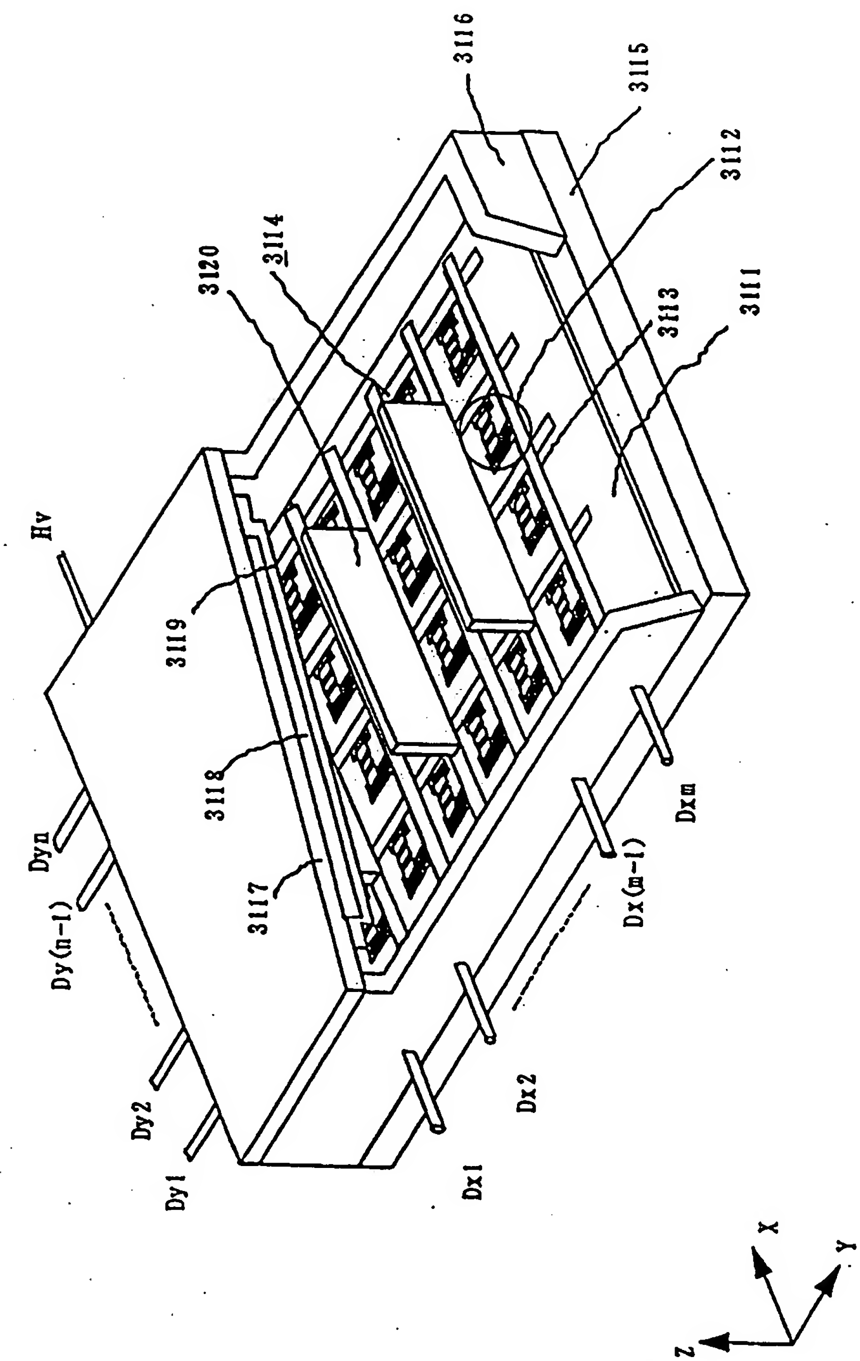
【図３４】 Fig. 34



【図３５】 Fig. 35



【図３６】 Fig. 36


3116
3115
3112
3114
3120
3113
3111
Hv
3119
3118
3117
Dyn
Dy(n-1)
Dy2
Dy1
Dxm
Dx(m-1)
Dx2
Dx1
X
Y
Z

[Name of the Document] Abstract

[Abstract]

[Problem(s)] A problem of the present invention is to provide a spacer, which controls static electrification, and an electron beam apparatus with high definition and long-term reliability in which displacement of emission points and creeping discharge involved with static electricity are restricted by providing the spacer.

[Means for Solving the Problem] In the electron beam apparatus comprising an electron source provided with electron emission devices, a face plate provided with anodes for accelerating the electrons emitted from the electron source, and spacers installed between the electron source and the face plate, wherein the incident angle dependency of secondary electron emission coefficient on the surface of the spacer is small, and incident energy of primary electron entering into the spacer surface is below the maximum, and when $\delta\theta$ and $\delta 0$ are the secondary electron emission coefficients against the primary electrons at incident angles of θ and 0 degrees respectively, the parameter m_0 in $\delta\theta/\delta 0 = (1/\cos\theta) \times \{1-\exp(-m_0\cos\theta)\}/\{1-\exp(-m_0)\}$ is 10 or smaller.

[Elected Drawing] Fig. 1

[Name of the Document]	Authorized Correction Data
[Document to be corrected]	Patent Application

<Recognition Information / Additional Information>

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[Attorney] Offeror

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1. Date of Change — August 30, 1990

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[Reason for Change]	New Registration
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